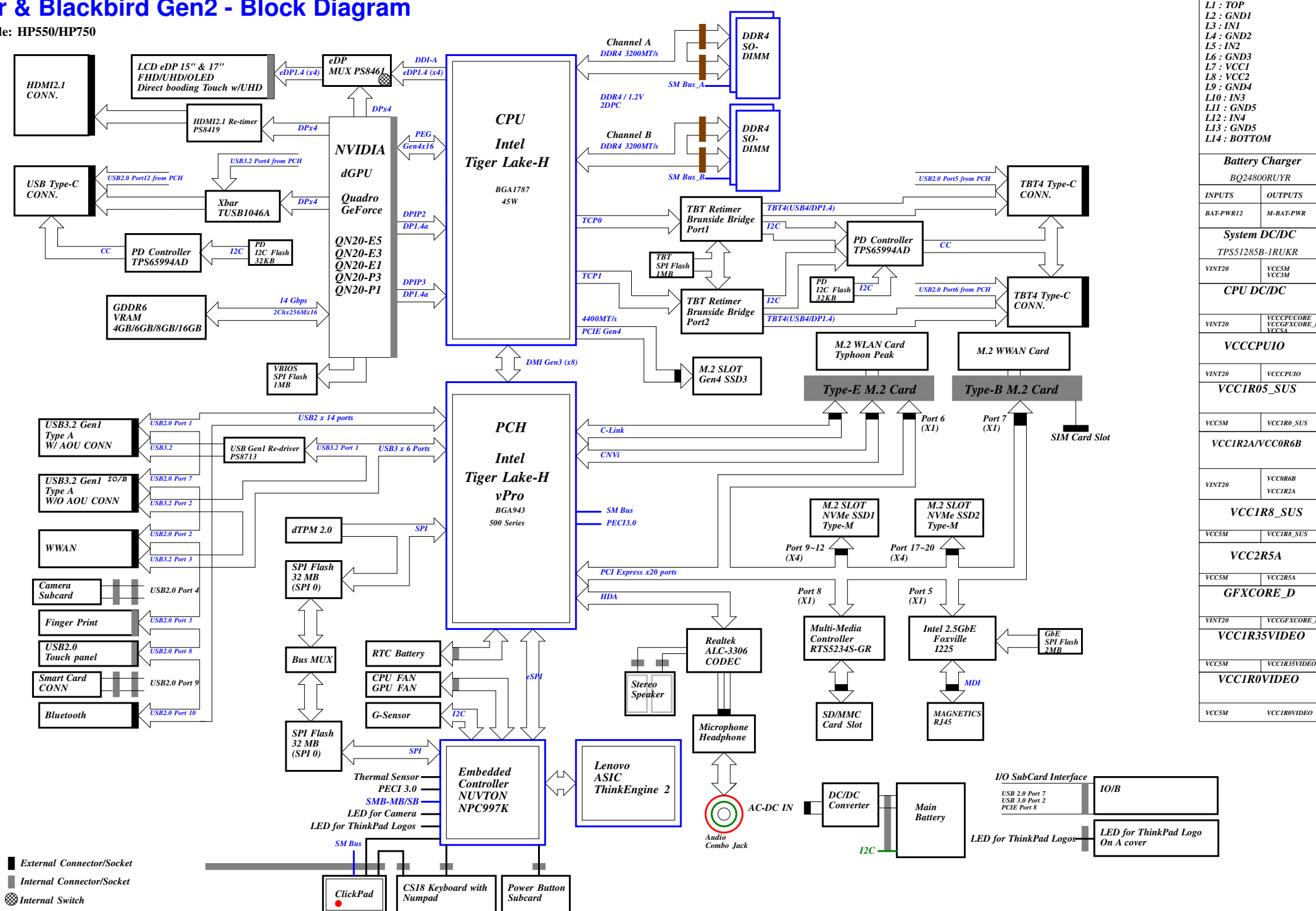


Raptor & Blackbird Gen2 Schematic Page Number

001_TITLE PAGE	047_THINK ENGINE 2(1/2)	093_Blank
002_BLOCK DIAGRAM	048_THINK ENGINE 2(2/2)	094_Blank
003_SYSTEM DEFINED	049_USB Type-A Port-A (AOU)	095_Blank
004_Power State	050_BLANK for TpPv USB Type-A	096_Blank
005_Power tree	051_G-Sensor/TPM2.0	097_Blank
006_CPU TGL-H: DDR4 CH-A	052_KB/Click PAD/Track Point/FP	098_Blank
007_CPU TGL-H: DDR4 CH-B	053_FAN/IOB CONN/AC-IN LED	099_Blank
008_CPU TGL-H: DDI/MISC/CLK/JTAG	054_SMB SW/Smart Card/eSPI Debug	100_Type C Adapter
009_CPU TGL-H: PCIE/DMI/TCP/DPIN	055_CardReader/SD Card for TpPv	101_DC-IN
010_CPU TGL-H: RSVD	056_MXM CONN	102_BATTERY INPUT
011_CPU TGL-H: POWER	057_Blank for TpPv GPU	103_BATTERY CHARGER
012_CPU TGL-H: GND	058_Blank for TpPv GPU	104_BLANK
013_PCH TGL-H: PCH Straps	059_Blank for TpPv GPU	105_DC/DC VCC5M/VCC3M
014_PCH TGL-H: CLK/CNVI/DMI	060_Blank for TpPv GPU	106_DC/DC VCC1R2A/VCC0R6B
015_PCH TGL-H: PCIE/USB/SPI/MISC	061_Blank for TpPv GPU	107_DC/DC VCC2R5A
016_PCH TGL-H: GPIO (1/2)	062_Blank for TpPv GPU	108_BLANK
017_PCH TGL-H: GPIO (2/2)	063_Blank for TpPv GPU	109_DC/DC IMVP9
018_PCH TGL-H: POWER	064_Blank for TpPv GPU	110_DC/DC VCCPUCORE
019_PCH TGL-H: GND	065_Blank for TpPv GPU	111_BLANK
020_RTC BATTERY/SPI FLASH/APS	066_Blank for TpPv GPU	112_BLANK
021_DDR4 CH-A PRIMARY	067_Blank for TpPv GPU	113_BLANK
022_DDR4 CH-A SECONDARY	068_Blank for TpPv GPU	114_VCCPUCORE DECOUPLING
023_DDR4 CH-B PRIMARY	069_Blank for TpPv GPU	115_VCCCPUCORE_AUX
024_DDR4 CH-B SECONDARY	070_Blank for TpPv GPU	116_VCCPCHCORE
025_THUNDERBOLT RETIMER A	071_SCREW HOLE	117_BLANK
026_THUNDERBOLT RETIMER B	072_Blank	118_BLANK
027_USB-C X-Bar	073_Blank	119_DC/DC VCC1R8_SUS
028_Type-C PD Controller-1 (TBT)	074_Blank	120_BLANK
029_Type-C PD Controller-2	075_Blank	121_DCDC_VCC12
030_TBT Type-C CONN	076_Blank	122_BLANK
031_USB Type-C CONN	077_Blank	123_BLANK
032_eDP Redriver	078_Blank	124_BLANK
033_LCD/Camera/Touch CONN	079_Blank	125_BLANK
034_HDMI2.1 Ret i ner and CONN	080_Blank	126_LOAD SW 1P8A
035_BLANK for TpPv HDMI LSPCON	081_Blank	127_LOAD SW VCC3_PD
036_M.2 NVMe SSD Slot_1&2	082_Blank	128_LOAD SW VCCST/VCCSTG
037_M.2 NVMe Gen4 SSD Slot_3	083_Blank	129_LOAD SW PCH SUS/TP
038_M.2 WLAN_2230	084_Blank	130_LOAD SW LAN
039_M.2 WWAN	085_Blank	131_LOAD SW B
040_Intel LAN (I225)	086_Blank	132_LOAD SW WWAN&WLAN
041_RJ45 CONN	087_Blank	133_LOAD SW VCC3_SSD
042_AUDIO SIP (ALC3306)	088_Blank	
043_HP/MIC/SPKR/Debug Port	089_Blank	
044_NPCX997KA0BX(1/3)	090_Blank	
045_NPCX997KA0BX(2/3)	091_Blank	
046_NPCX997KA0BX(3/3)	092_Blank	

Raptor & Blackbird Gen2 - Block Diagram

Project Code: HP550/HP750



PCB Layer Stackup	
L1 :	TOP
L2 :	GND1
L3 :	IN1
L4 :	GND2
L5 :	IN2
L6 :	GND3
L7 :	VCC1
L8 :	VCC2
L9 :	GND4
L10 :	IN3
L11 :	GND5
L12 :	IN4
L13 :	GND5
L14 :	BOTTOM

Battery Charger	
BQ24800RUYR	
INPUTS	OUTPUTS
BAT-PWR12	M-BAT-PWR

System DC/DC	
TPS51285B-1RU/KR	
VINT20	VCC5M
VINT20	VCC3M

CPU DC/DC	
VINT20	VCCCPUCORE
VINT20	VCCGFXCORE_1
VINT20	VCC3A

VCCCPU10	
VINT20	VCCCPU10

VCC1R05_SUS	
VCC5M	VCC1R05_SUS

VCC1R2A/VCC0R6B	
VINT20	VCC0R6B
VINT20	VCC1R2A

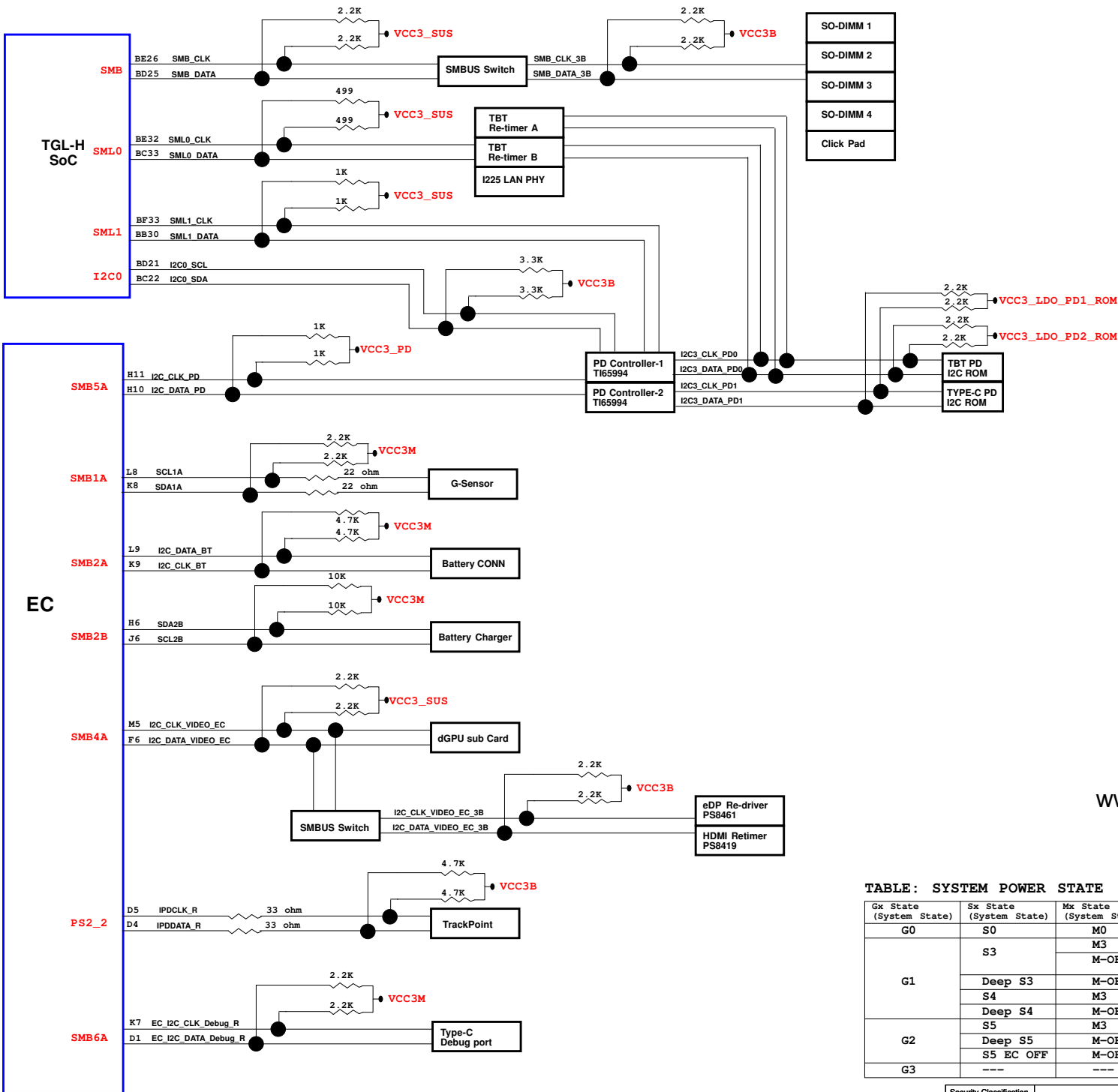
VCC1R8_SUS	
VCC5M	VCC1R8_SUS

VCC2R5A	
VCC5M	VCC2R5A

GFXCORE_D	
VINT20	VCCGFXCORE_D

VCC1R35VIDEO	
VCC5M	VCC1R35VIDEO

VCC1R0VIDEO	
VCC5M	VCC1R0VIDEO



PCH SM Bus address

Device	Address	Device	Address
CH-A P	DDR DIMM0	TBT Re-timer A	0x20h
CH-A S	DDR DIMM1	TBT Re-timer B	0x21h
CH-B P	DDR DIMM2	Intel Lan_I225	0x49h
CH-B S	DDR DIMM3		

PCH SM L1 address

Device	Address	Port	Device	Address	Port
Power Delivery (Ti65994)	0x23h	TBT Port A (JTBT1)	Power Delivery (Ti65994)	0x21h	Planar Type-C (JUSBC1)
Power Delivery (Ti65994)	0x27h	TBT Port B (JTBT2)			
Power Delivery (Ti65994)	0x21h	Planar Type-C (JUSBC1)			

EC SMBus5 address

Device	Address	Port
Power Delivery (Ti65994)	0x20h	TBT Port A (JTBT1)
Power Delivery (Ti65994)	0x24h	TBT Port B (JTBT2)
Power Delivery (Ti65994)	0x21h	Planar Type-C (JUSBC1)

EC SMBus1 address

Device	Address
G-Sensor (LIS2DWLTR)	0x30h (W) / 0x31h (R)
G-Sensor (BMA280)	0x30h (W) / 0x31h (R)

ST and Bosch I2C address is same but can be identified by chip ID

EC SMBus4 address

Device	Address
DGPU	0x9Eh
eDP Re-driver PS8461	0x10h-0x2Fh
HDMI Retimer PS8419	0x30h-0x4Fh

PD I2C3m address

Device	Address
TBT Re-timer A	0x52
TBT Re-timer B	0x51
TBT PD I2C ROM	0x50
TYPE-C PD I2C ROM	0x50

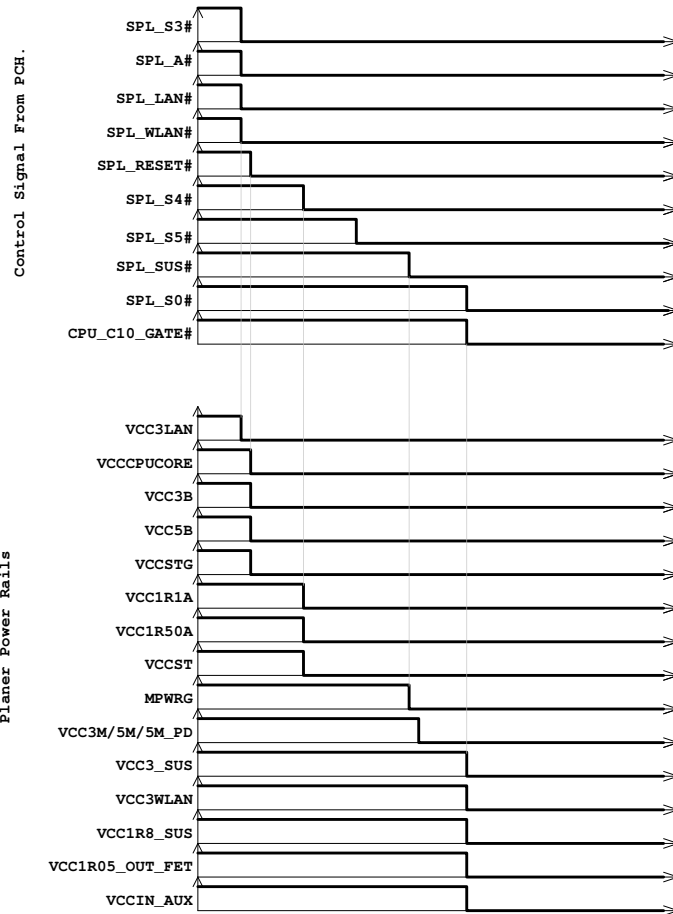
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TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	MT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	Suspend-to-Disk (STD)
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	
G2	Deep S4	M-OFF	ON	ON	OFF	OFF	OFF	OFF		
	S5	M3	ON	ON	ON	ON	OFF	OFF	Hibernation or Shutdown	Soft Off
	Deep S5	M-OFF	ON	ON	OFF	OFF	OFF	OFF		
G3	S5 EC OFF	M-OFF	OFF	OFF	OFF	OFF	OFF	OFF		
G3	---	---	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off

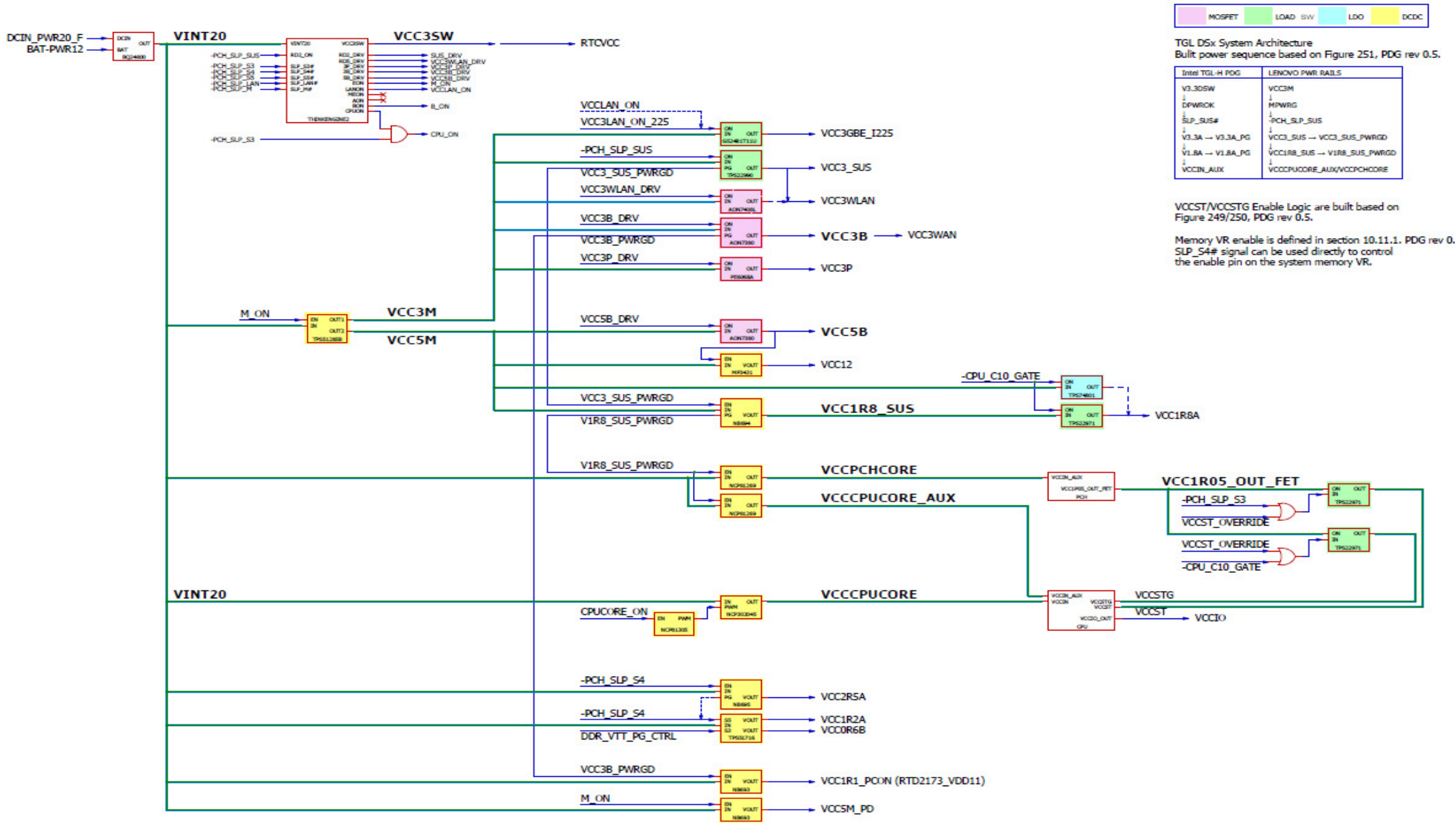
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Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd		SYSTEM DEFINED
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					Document Number Raptor & Blackbird Gen2
					Rev 0.4
					Date: Thursday, April 25, 2021
					Sheet 3 of 13

Timing Diagram for S0/M0 to G3 [Deep Sx]
Based on planer power rail.



Power Rail Name	Voltage Range	Enable/Control Signal	Sx Power State			
			S0	S3	S4	S5
VINT20	9-20V	NA	ON	ON	ON	ON
RTCVCC	3-3.3V	NA	ON	ON	ON	ON
VCC3SW	3.3V	NA	ON	ON	ON	ON
VCC3M	3.3V	M_ON	ON	ON	ON	ON
VCC3LAN	3.3V	VCC3LAN_DRV	ON	OFF	OFF	OFF
VCC3_SUS	3.3V	SUS_DRV	ON	ON	ON	ON
VCC3WLAN	3.3V	NA	ON	ON	ON	ON
VCC3B	3.3V	VCC3B_DRV	ON	OFF	OFF	OFF
VCC3P	3.3V	VCC3P_DRV	ON	OFF	OFF	OFF
VCC5M	5V	M_ON	ON	ON	ON	ON
VCC5B	5V	VCC5B_DRV	ON	OFF	OFF	OFF
VCC1R8_SUS	1.8V	VCC3_SUS-PWRGD	ON	ON	ON	ON
VCC1R8A	1.8V	-CPU_C10_GATE	ON	ON	ON	ON
VCCPCHCORE	2 bit VID	V1R8_SUS_PWRGD	ON	ON	ON	ON
VCCST	1.05V	VCCST_OVERRIDE OR -PCH_SLP_S3	ON	OFF	OFF	OFF
VCCSTG	1.05V	VCCST_OVERRIDE OR -CPU_C10_GATE	ON	OFF	OFF	OFF
VCCCPUCORE	SVID	CPUCORE_ON	ON	OFF	OFF	OFF
VCC1R1A	1.1V	-PCH_SLP_S4	ON	ON	OFF	OFF
VCC5R0A	5V	-PCH_SLP_S4*	ON	ON	OFF	OFF
VCC5M_PD	5V	M_ON	ON	ON	ON	ON
VCC1R1_PCON	1.1V	TBD				

Not fixed yet.
Please refer to latest TGL-H PDG.



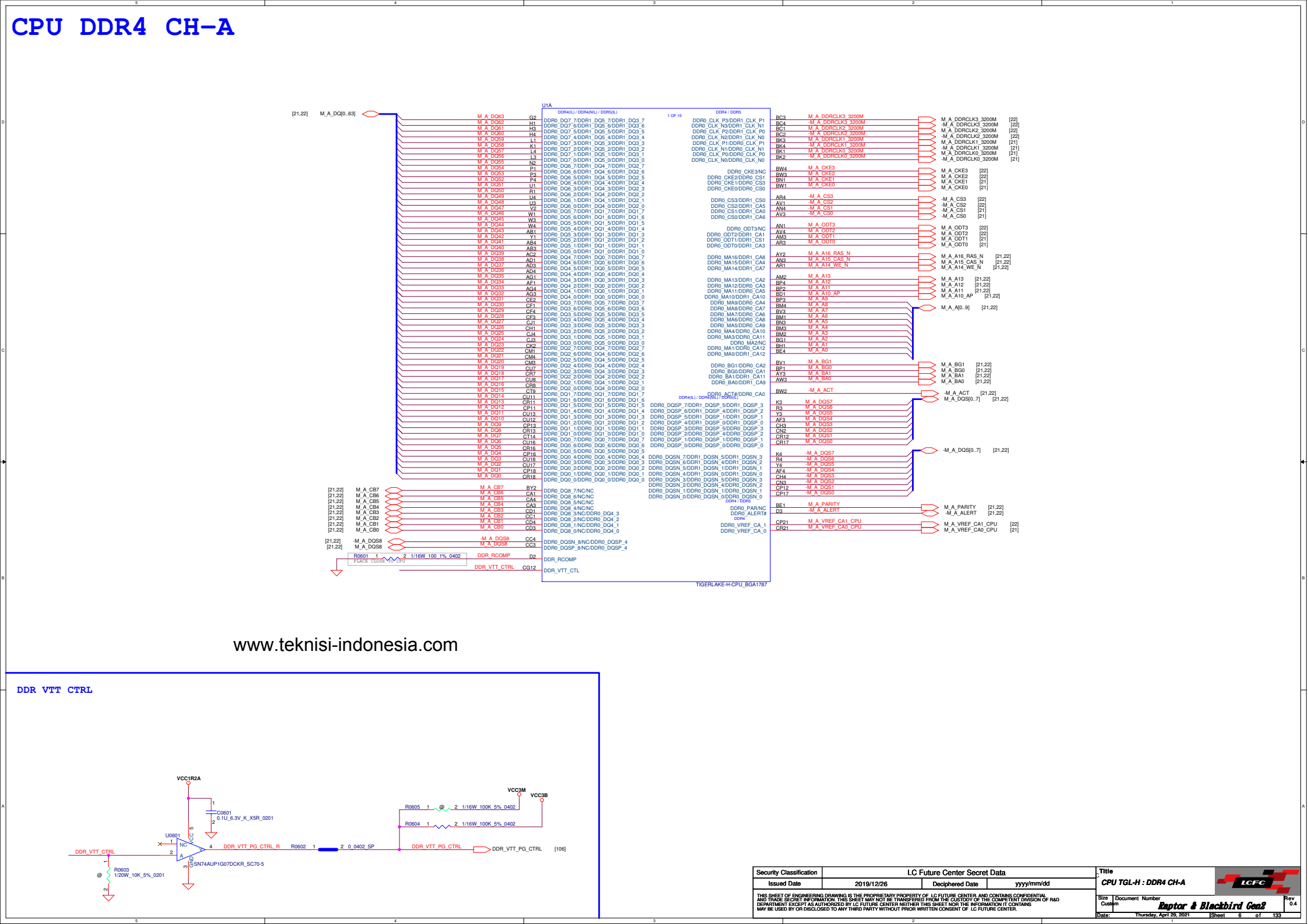
Power Tree

[illegible][illegible]

CPU DDR4 CH-A


The diagram illustrates the electrical connections for the CPU's DDR4 Channel A. It shows a dense array of pins on the left, each connected to a specific component or signal path. Key components include:

- Resistors:** R0601, R0602, R0603, R0604, R0605, R0606, R0607, R0608, R0609, R0610, R0611, R0612, R0613, R0614, R0615, R0616, R0617, R0618, R0619, R0620, R0621, R0622, R0623, R0624, R0625, R0626, R0627, R0628, R0629, R0630, R0631, R0632, R0633, R0634, R0635, R0636, R0637, R0638, R0639, R0640, R0641, R0642, R0643, R0644, R0645, R0646, R0647, R0648, R0649, R0650, R0651, R0652, R0653, R0654, R0655, R0656, R0657, R0658, R0659, R0660, R0661, R0662, R0663, R0664, R0665, R0666, R0667, R0668, R0669, R0670, R0671, R0672, R0673, R0674, R0675, R0676, R0677, R0678, R0679, R0680, R0681, R0682, R0683, R0684, R0685, R0686, R0687, R0688, R0689, R0690, R0691, R0692, R0693, R0694, R0695, R0696, R0697, R0698, R0699, R0700, R0701, R0702, R0703, R0704, R0705, R0706, R0707, R0708, R0709, R0710, R0711, R0712, R0713, R0714, R0715, R0716, R0717, R0718, R0719, R0720, R0721, R0722, R0723, R0724, R0725, R0726, R0727, R0728, R0729, R0730, R0731, R0732, R0733, R0734, R0735, R0736, R0737, R0738, R0739, R0740, R0741, R0742, R0743, R0744, R0745, R0746, R0747, R0748, R0749, R0750, R0751, R0752, R0753, R0754, R0755, R0756, R0757, R0758, R0759, R0760, R0761, R0762, R0763, R0764, R0765, R0766, R0767, R0768, R0769, R0770, R0771, R0772, R0773, R0774, R0775, R0776, R0777, R0778, R0779, R0780, R0781, R0782, R0783, R0784, R0785, R0786, R0787, R0788, R0789, R0790, R0791, R0792, R0793, R0794, R0795, R0796, R0797, R0798, R0799, R0800, R0801, R0802, R0803, R0804, R0805, R0806, R0807, R0808, R0809, R0810, R0811, R0812, R0813, R0814, R0815, R0816, R0817, R0818, R0819, R0820, R0821, R0822, R0823, R0824, R0825, R0826, R0827, R0828, R0829, R0830, R0831, R0832, R0833, R0834, R0835, R0836, R0837, R0838, R0839, R0840, R0841, R0842, R0843, R0844, R0845, R0846, R0847, R0848, R0849, R0850, R0851, R0852, R0853, R0854, R0855, R0856, R0857, R0858, R0859, R0860, R0861, R0862, R0863, R0864, R0865, R0866, R0867, R0868, R0869, R0870, R0871, R0872, R0873, R0874, R0875, R0876, R0877, R0878, R0879, R0880, R0881, R0882, R0883, R0884, R0885, R0886, R0887, R0888, R0889, R0890, R0891, R0892, R0893, R0894, R0895, R0896, R0897, R0898, R0899, R0900, R0901, R0902, R0903, R0904, R0905, R0906, R0907, R0908, R0909, R0910, R0911, R0912, R0913, R0914, R0915, R0916, R0917, R0918, R0919, R0920, R0921, R0922, R0923, R0924, R0925, R0926, R0927, R0928, R0929, R0930, R0931, R0932, R0933, R0934, R0935, R0936, R0937, R0938, R0939, R0940, R0941, R0942, R0943, R0944, R0945, R0946, R0947, R0948, R0949, R0950, R0951, R0952, R0953, R0954, R0955, R0956, R0957, R0958, R0959, R0960, R0961, R0962, R0963, R0964, R0965, R0966, R0967, R0968, R0969, R0970, R0971, R0972, R0973, R0974, R0975, R0976, R0977, R0978, R0979, R0980, R0981, R0982, R0983, R0984, R0985, R0986, R0987, R0988, R0989, R0990, R0991, R0992, R0993, R0994, R0995, R0996, R0997, R0998, R0999, R1000, R1001, R1002, R1003, R1004, R1005, R1006, R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014, R1015, R1016, R1017, R1018, R1019, R1020, R1021, R1022, R1023, R1024, R1025, R1026, R1027, R1028, R1029, R1030, R1031, R1032, R1033, R1034, R1035, R1036, R1037, R1038, R1039, R1040, R1041, R1042, R1043, R1044, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053, R1054, R1055, R1056, R1057, R1058, R1059, R1060, R1061, R1062, R1063, R1064, R1065, R1066, R1067, R1068, R1069, R1070, R1071, R1072, R1073, R1074, R1075, R1076, R1077, R1078, R1079, R1080, R1081, R1082, R1083, R1084, R1085, R1086, R1087, R1088, R1089, R1090, R1091, R1092, R1093, R1094, R1095, R1096, R1097, R1098, R1099, R1100, R1101, R1102, R1103, R1104, R1105, R1106, R1107, R1108, R1109, R1110, R1111, R1112, R1113, R1114, R1115, R1116, R1117, R1118, R1119, R1120, R1121, R1122, R1123, R1124, R1125, R1126, R1127, R1128, R1129, R1130, R1131, R1132, R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1143, R1144, R1145, R1146, R1147, R1148, R1149, R1150, R1151, R1152, R1153, R1154, R1155, R1156, R1157, R1158, R1159, R1160, R1161, R1162, R1163, R1164, R1165, R1166, R1167, R1168, R1169, R1170, R1171, R1172, R1173, R1174, R1175, R1176, R1177, R1178, R1179, R1180, R1181, R1182, R1183, R1184, R1185, R1186, R1187, R1188, R1189, R1190, R1191, R1192, R1193, R1194, R1195, R1196, R1197, R1198, R1199, R1200, R1201, R1202, R1203, R1204, R1205, R1206, R1207, R1208, R1209, R1210, R1211, R1212, R1213, R1214, R1215, R1216, R1217, R1218, R1219, R1220, R1221, R1222, R1223, R1224, R1225, R1226, R1227, R1228, R1229, R1230, R1231, R1232, R1233, R1234, R1235, R1236, R1237, R1238, R1239, R1240, R1241, R1242, R1243, R1244, R1245, R1246, R1247, R1248, R1249, R1250, R1251, R1252, R1253, R1254, R1255, R1256, R1257, R1258, R1259, R1260, R12

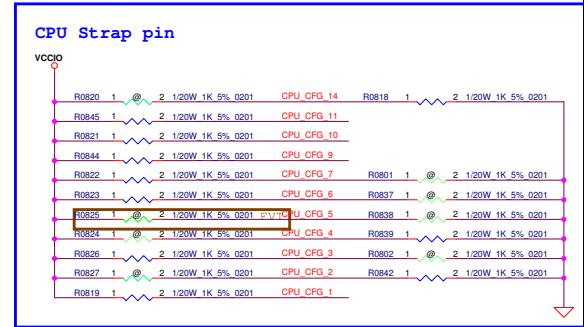
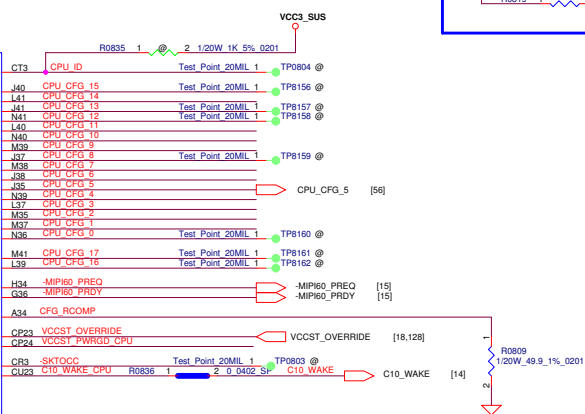
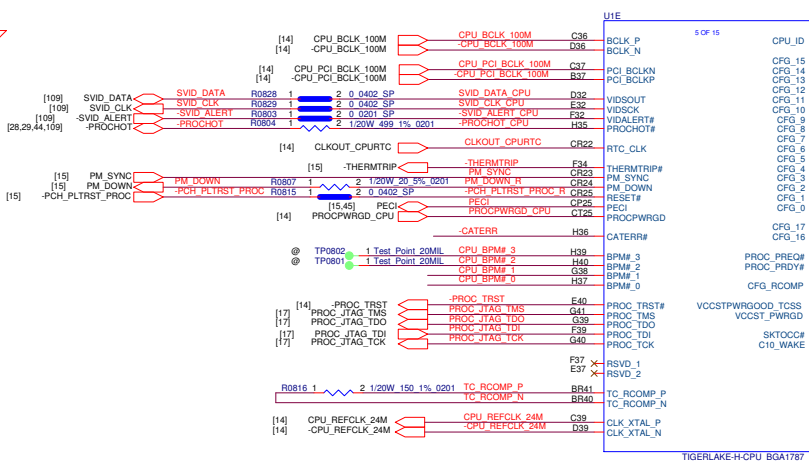
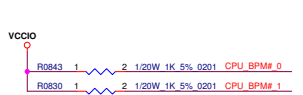
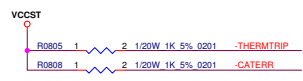
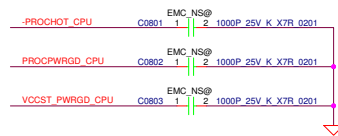
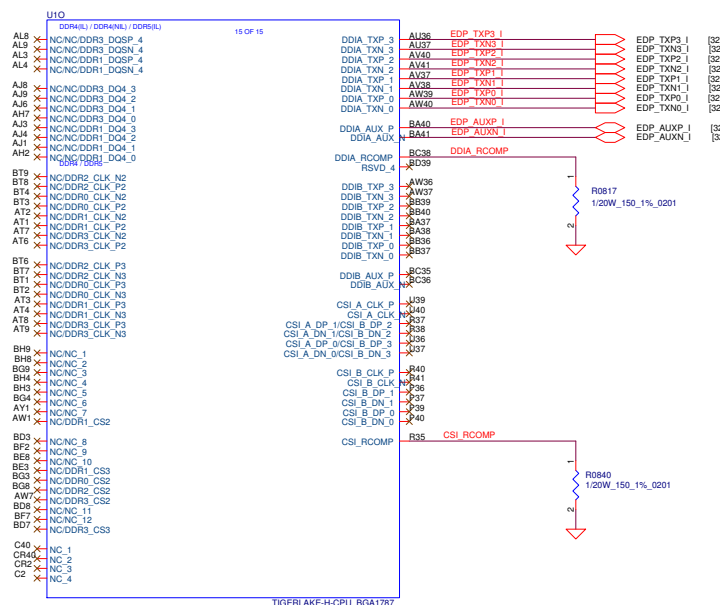
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CPU DDR4 CH-B

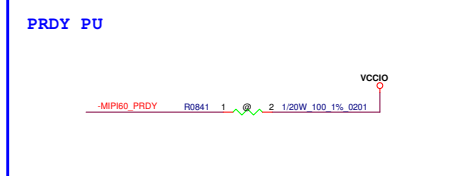
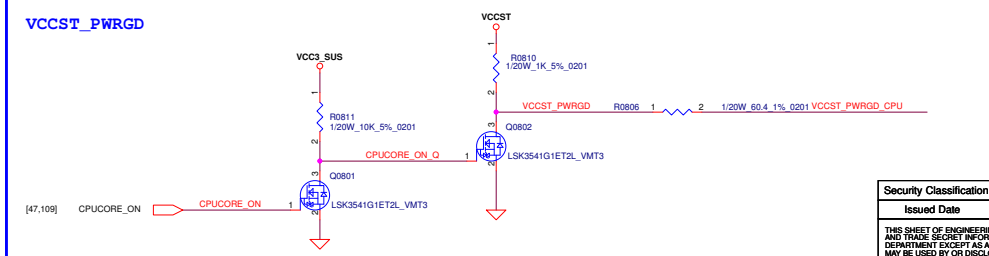


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				Customer	Raptor & Blackbird Gen2	
				Date:	Thursday, April 28, 2021	Sheet


CPU DDI/MISC/CLK/JTAG



CFG pin assignment	
0	RSVD
1	RSVD(Pull-up)
2	PEG x16 Lane Reversal 1:Normal 0:Reversed <----- Logic
3	RSVD(Pull-up)
4	eDP enable 0:Enabled <----- Logic 1:Disabled
6:5	PCI Express Bifurcation 00: 1x8, 2x4 PCI Express 01: Reserved 10: 2x8 PCI Express <----- QN20P 11:1x16 PCI Express <----- QN20E
7	PEG Deferred Link Training 1:Enabled <----- Logic 0:Disabled
8	RSVD
11:9	RSVD(Pull-up)
13:12	RSVD
14	PEG60(PCIe4) Lane Reversal 1:Normal 0:Reversed <----- Logic <----- Reversed on Module side (JMSD3)
17:15	RSVD



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CPU POWER

VCCPUCORE
VCCPUCORE_AUX
VCCIO
VCC1R2A

TIGERLAKE-H-CPU_BGA1787

TIGERLAKE-H-CPU_BGA1787

TIGERLAKE-H-CPU_BGA1787

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Security Classification	LC Future Center Secret Data			Title
Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	CPU TGL-H : POWER
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Rev	0.4	Date	Thursday, April 25, 2021	Sheet 11 of 153

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The image is a technical drawing of a CPU power distribution system, specifically for the TIGERLAKE-H-CPU_BGA1787. It consists of a main schematic at the top and several detailed sub-circuits at the bottom.

Main Schematic:

- Power Planes:** VCCPUCORE, VCCPUCORE_AUX, VCC1R2A.
- Decoupling Capacitors:** Numerous capacitors are shown, including 100nF, 10uF, and 100uF types, distributed across the power planes.
- Signal Lines:** Various signal lines are shown, including VCCIO, VCCST, VCCSTG, VCCSTG_TERM, VCC1R2A, and VCCPUCORE_AUX.
- Resistors:** Resistors are shown in series with the power lines, including 100k, 1k, and 10k types.
- Labels:** The main schematic is labeled "TIGERLAKE-H-CPU_BGA1787".

Sub-Circuits:

- VCCST:** A detailed circuit for the VCCST power rail, showing a 100nF capacitor and a 10uF capacitor.
- VCC1R2A:** A detailed circuit for the VCC1R2A power rail, showing a 100nF capacitor and a 10uF capacitor.
- VCCPUCORE_AUX:** A detailed circuit for the VCCPUCORE_AUX power rail, showing a 100nF capacitor and a 10uF capacitor.
- VCCPUCORE:** A detailed circuit for the VCCPUCORE power rail, showing a 100nF capacitor and a 10uF capacitor.

Title Block:

The title block is located at the bottom right of the drawing and contains the following information:

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- Title:** CPU TGL-H : POWER
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- Sheet:** 11 of 153

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- VCCPUCORE:** A detailed circuit for the VCCPUCORE power rail, showing a 100nF capacitor and a 10uF capacitor.

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CPU GND

Diagram illustrating the CPU Ground (GND) connections for the TigerLake-H-CPU BGA1787, showing various NCTF CPU pins and their corresponding ground connections.

The diagram is divided into four main sections, each representing a different NCTF CPU pin:

- NCTF CPU A1 A3:** Shows connections for pins A11 through A39, including ground connections for various NCTF CPU pins (e.g., A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39).
- NCTF CPU A1 A4:** Shows connections for pins A41 through A49, including ground connections for various NCTF CPU pins (e.g., A41, A42, A43, A44, A45, A46, A47, A48, A49).
- NCTF CPU A1 A5:** Shows connections for pins A51 through A59, including ground connections for various NCTF CPU pins (e.g., A51, A52, A53, A54, A55, A56, A57, A58, A59).
- NCTF CPU A1 A6:** Shows connections for pins A61 through A69, including ground connections for various NCTF CPU pins (e.g., A61, A62, A63, A64, A65, A66, A67, A68, A69).

The diagram also includes a detailed view of the TigerLake-H-CPU BGA1787 package, showing the various pins and their corresponding ground connections. The package is labeled "TIGERLAKE-H-CPU BGA1787" and "TIGERLAKE-H-CPU BGA1787".

Corner NCTF test pin

NCTF CPU	Test Point	20MIL	1	TP1201 @	NCTF CPU	Test Point	20MIL	1	TP1202 @
NCTF CPU A1 A3	Test Point 20MIL	1	TP1201 @	NCTF CPU A1 A4	Test Point 20MIL	1	TP1202 @		
NCTF CPU A1 A4	Test Point 20MIL	1	TP1206 @	NCTF CPU A1 A5	Test Point 20MIL	1	TP1203 @		
NCTF CPU A1 A5	Test Point 20MIL	1	TP1207 @	NCTF CPU A1 A6	Test Point 20MIL	1	TP1204 @		
NCTF CPU A1 A6	Test Point 20MIL	1	TP1210 @	NCTF CPU A1 A7	Test Point 20MIL	1	TP1205 @		
NCTF CPU A1 A7	Test Point 20MIL	1	TP1209 @	NCTF CPU A1 A8	Test Point 20MIL	1	TP1216 @		
NCTF CPU A1 A8	Test Point 20MIL	1	TP1208 @	NCTF CPU A1 A9	Test Point 20MIL	1	TP1215 @		
NCTF CPU A1 A9	Test Point 20MIL	1	TP1211 @	NCTF CPU A1 A10	Test Point 20MIL	1	TP1214 @		
NCTF CPU A1 A10	Test Point 20MIL	1	TP1212 @	NCTF CPU A1 A11	Test Point 20MIL	1	TP1213 @		
NCTF CPU A1 A11	Test Point 20MIL	1	TP1220 @	NCTF CPU A1 A12	Test Point 20MIL	1	TP1217 @		
NCTF CPU A1 A12	Test Point 20MIL	1	TP1218 @						
NCTF CPU A1 A13	Test Point 20MIL	1	TP1219 @						
NCTF CPU A1 A14	Test Point 20MIL	1	TP1221 @						
NCTF CPU A1 A15	Test Point 20MIL	1	TP1222 @						

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Title CPU TGL-H : GND

Size Document Number **Rev** 0.4

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ICFC **Raptor & Blackbird Gen2**

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CPU GND

Diagram illustrating the CPU Ground (GND) connections for the TigerLake-H-CPU BGA1787, showing various NCTF CPU pins and their corresponding GND connections.

The diagram is divided into four main sections, each representing a different NCTF CPU pin:

- NCTF CPU A1 A3:** Shows connections for pins A11 through A39, including NCTF CPU A1 A3, NCTF CPU A1 A37, NCTF CPU A1 A4, and NCTF CPU A1 A5.
- NCTF CPU A1 B2:** Shows connections for pins B1 through B10, including NCTF CPU A1 B2 and NCTF CPU A1 B41.
- NCTF CPU C1 C1:** Shows connections for pins C1 through C10, including NCTF CPU C1 C1 and NCTF CPU C1 C2.
- NCTF CPU C1 C2:** Shows connections for pins C11 through C20, including NCTF CPU C1 C1, NCTF CPU C1 C2, and NCTF CPU C1 C3.

The diagram also includes a detailed view of the TigerLake-H-CPU BGA1787 package, showing the various pins and their corresponding GND connections.

Corner NCTF test pin

NCTF CPU	Test Point	TP
NCTF CPU C1 C1	Test Point 20MIL 1	TP1201
NCTF CPU C1 C2	Test Point 20MIL 1	TP1202
NCTF CPU C1 C3	Test Point 20MIL 1	TP1203
NCTF CPU C1 C4	Test Point 20MIL 1	TP1204
NCTF CPU A1 A3	Test Point 20MIL 1	TP1205
NCTF CPU A1 A37	Test Point 20MIL 1	TP1206
NCTF CPU A1 A4	Test Point 20MIL 1	TP1207
NCTF CPU A1 A5	Test Point 20MIL 1	TP1208
NCTF CPU A1 B2	Test Point 20MIL 1	TP1209
NCTF CPU A1 B41	Test Point 20MIL 1	TP1210
NCTF CPU C1 C1	Test Point 20MIL 1	TP1211
NCTF CPU C1 C2	Test Point 20MIL 1	TP1212
NCTF CPU C1 C3	Test Point 20MIL 1	TP1213
NCTF CPU C1 C4	Test Point 20MIL 1	TP1214
NCTF CPU A1 A3	Test Point 20MIL 1	TP1215
NCTF CPU A1 A37	Test Point 20MIL 1	TP1216
NCTF CPU A1 A4	Test Point 20MIL 1	TP1217
NCTF CPU A1 A5	Test Point 20MIL 1	TP1218
NCTF CPU A1 B2	Test Point 20MIL 1	TP1219
NCTF CPU A1 B41	Test Point 20MIL 1	TP1220
NCTF CPU C1 C1	Test Point 20MIL 1	TP1221
NCTF CPU C1 C2	Test Point 20MIL 1	TP1222

Security Classification
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LC Future Center Secret Data

Title
CPU TGL-H : GND

Rev
0.4

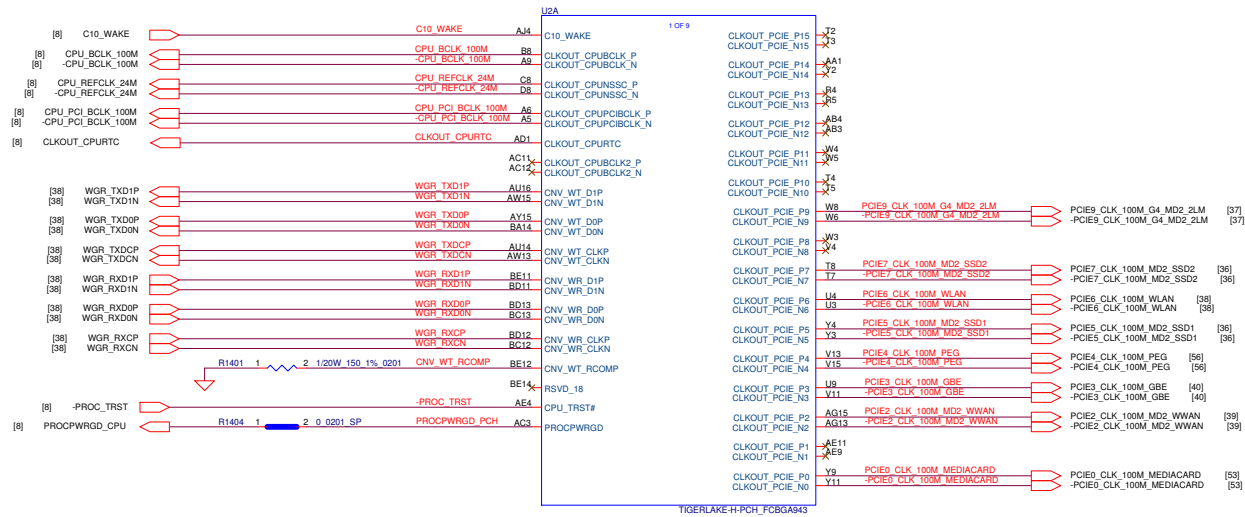
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PCH Straps

Reference 615985-tgl-rkl-pch-eds-vol1-rev0p7, Table17

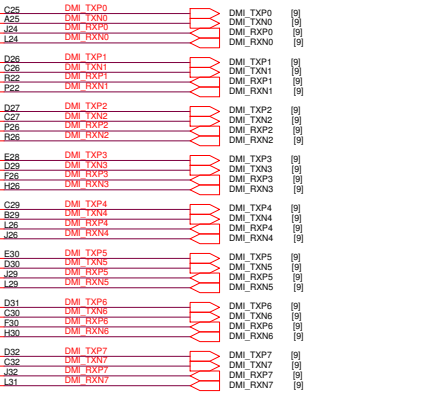
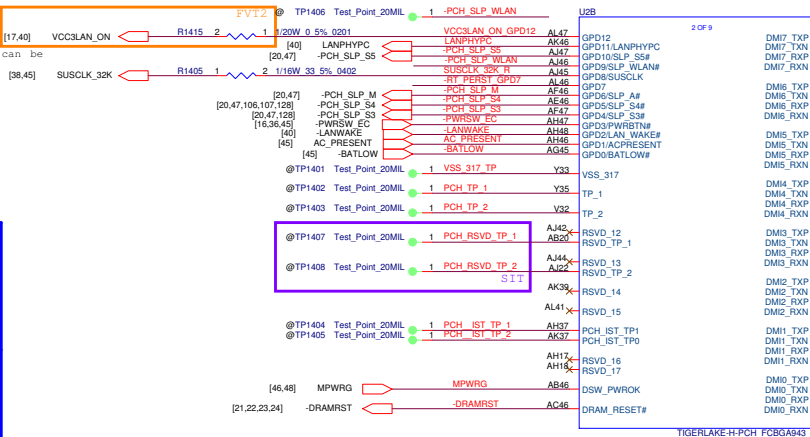
Signal	Usage	Comment	Setting
GPP_B14/SPKR	Top Swap Override	0 = Disable "TOP Swap" Mode (Default) 1 = Enable "TOP Swap" Mode <small>This strap has a 20k internal PD</small>	This strap is set by EC. See "BIOS_HEALING" signal
GPP_B18/GSPI0_MOSI	No Reboot	0 = Disable "No Reboot" Mode (Default) ← Logic 1 = Enable "No Reboot" Mode <small>This strap has a 20k internal PD</small>	[17] GPP_B18_NO_REBOOT GPP_B18_NO_REBOOT R1305 1 2 1/20W 1K 5% 0201 VCC3_SUS
GPP_C2/SMBALERT#	TLS Confidentiality	0 = Disable ME Crypto TLS(Default) 1 = Enable ME Crypto TLS with Confidentiality ← Logic <small>This strap has a 20k internal PD</small>	[17] GPP_C2 GPP_C2 R1302 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
GPP_C5/SML0ALERT#	eSPI Disable	0 = Enable eSPI (Default) ← Logic 1 = Disable eSPI <small>This strap has a 20k internal PD</small>	[17] GPP_C5 GPP_C5 R1310 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
SPI0_MOSI	Reserved	External pull-up is required Recommend 4.7K PU	[15,20,51] SPI_MOSI_I00 SPI_MOSI_I00 R1308 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
GPP_G9/ISH_SPI_CLK/ DDP3_CTRLDATA/ GSPi2_CLK/ TBT_LSX2_RXD	DDP3 I2C/TBT_LSX2/ BBSB_LS2 pins VCC configuration	0 = DDP3 I2C/TBT_LSX2/BBSB_LS2 pins at 1.8V ← Logic 1 = DDP3 I2C/TBT_LSX2/BBSB_LS2_TX pins at 3.3V <small>This strap has a 20k internal PD</small>	NC
GPP_G11/ ISH_SPI_MOSI/ DDP4_CTRLDATA/ GSPi2_MOSI/ TBT_LSX3_RXD	DDP4 I2/TBT_LSX3/ BSSB_LS3 pins VCC configuration	0 = DDP4 I2C/TBT_LSX3/BBSB_LS3 pins at 1.8V ← Logic 1 = DDP4 I2C/TBT_LSX3/BBSB_LS3 pins at 3.3V <small>This strap has a 20k internal PD</small>	NC
GPP_B23/ SML1ALERT#/ PCHHOT#	CPUNSSC Clock Frequency	0 = 38.4 MHz clock (direct from crystal) (Default) ← Logic 1 = 19.2 MHz clock (derived from 38.4 MHz crystal) <small>This strap has a 20k internal PD</small>	[17] GPP_B23 GPP_B23 R1301 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
SPI0_IO2	Reserved	External pull-up is required ← Logic Recommend 100K if pulled up to 3.3V	[15,20] SPI_IO2 SPI_IO2 R1307 1 2 1/20W 100K 5% 0201 VCC3_SUS
SPI0_IO3	Reserved	External pull-up is required ← Logic Recommend 100K if pulled up to 3.3V	[15,20] SPI_IO3 SPI_IO3 R1306 1 2 1/20W 100K 5% 0201 VCC3_SUS
GPP_R2 / HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	0 = Enable security measures defined in the Flash Descriptor (Default) 1 = Disable Flash Descriptor Security (override) <small>This strap has a 20k internal PD</small>	<div>PLACE ON BOTTOM SIDE</div> <div>TEST PAD BOTTOM SIDE DO NOT MOVE AFTER FIX</div> <div>vcc3_sus</div> <div>R1303 1 2 1/20W 1K 5% 0201</div> <div>911 9453 R1304 1 2 1/20W 0.5% 0201</div> <div>Test Point 20MIL</div> <div>TP1301</div> <div>Test Point 20MIL</div> <div>TP1302</div> <div>HDA_SDO_R</div> <div>HDA_SDO_R [19]</div>
GPP_H12/ SML2ALERT#	eSPI Flash Sharing Mode	0 = Master Attached Flash Sharing (MAFS) enabled ← Logic (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled <small>This strap has a 20k internal PD</small>	[16] GPP_H12 GPP_H12 R1312 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
GPP_H15 / SML3ALERT#	JTAG ODT Disable	0 = JTAG ODT is disabled (Default) 1 = JTAG ODT is enabled ← Logic <small>This strap has a 20k internal PD</small>	[16] GPP_H15 GPP_H15 R1309 1 2 1/20W 100K 5% 0201 VCC3_SUS
GPP_H18 / SML4ALERT#	VCCSPI Voltage Configuration	0 = VCCSPI at 3.3 V (Default) ← Logic 1 = VCCSPI at 1.8 V <small>This strap has a 20k internal PD</small>	[16] GPP_H18 GPP_H18 R1313 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
GPP_G13 / DDP1_CTRLDATA / TBT_LSX0_RXD	DDP1 I2C/TBT_LSX0 /BSSB_LS0 pins VCC configuration	0 = DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V ← Logic 1 = DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V <small>This strap has a 20k internal PD</small>	[17,25] TBT_LSX0_RXD TBT_LSX0_RXD R1311 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
GPP_G15 / DDP2_CTRLDATA / TBT_LSX1_RXD	DDP2 I2C / TBT_LSX1 /BSSB_LS01pins VCC configuration	0 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 1.8V ← Logic 1 = DDP2 I2C / TBT_LSX1 / BSSB_LS1 pins at 3.3V <small>This strap has a 20k internal PD</small>	[17,26] TBT_LSX1_RXD TBT_LSX1_RXD R1314 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
DBG_PMODE	Reserved	This strap should sample high <small>This strap has a 20k internal PU</small>	NC
GPP_J2 / CNV_BRI_DT / UART0_RTS#	XTAL_Frequency Selection	0 = 38.4 MHz (Default) ← Logic 1 = 24 MHz <small>This strap has a 20k internal PD</small>	[16] BRI_DT_CNVI_R BRI_DT_CNVI_R R1316 1 2 1/20W 20K 5% 0201 VCC1R8_SUS PD exists in WLAN page (not for strap function)
GPP_J4 / CNV_RGI_DT / UART0_TXD	M.2 CNVi Mode Select	0 = Integrated CNVi enabled ← CNVi 1 = Integrated CNVi disabled ← Discrete <small>This strap doesn't have an internal PU or PD. A weak external pull-up is required.</small>	PU exists in WLAN page It should be near the WLAN M.2 CNVi module has PD and strap value changes depends on type of module
GPP_B22 / GSPi1_MOSI	Boot BIOS Strap (BBS)	0 = BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF) ← Logic 1 = BIOS fetches are routed to the eSPI Peripheral Channel <small>This strap has a 20k internal PD</small>	[17] GPP_B22 GPP_B22 R1315 1 2 1/20W 4.7K 5% 0201 VCC3_SUS
GPD7	Reserved	This strap should sample LOW <small>This strap has a 20k internal PD</small>	NC(Used only as GPIO)

PCH CLK/CNVI/DMI



CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] =
Must be used for PCIe* Gen4 support

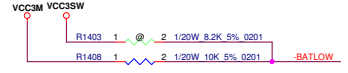
SUSCLK
0 ohm placeholder is recommended, but not mandatory.
If failing device Over/Undershoot, a 33 ohm resistor can be
stuffed.



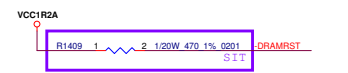
LAN_WAKE# PU



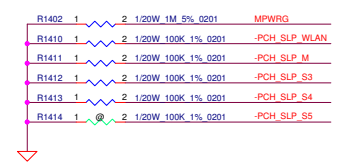
-BATLOW PU



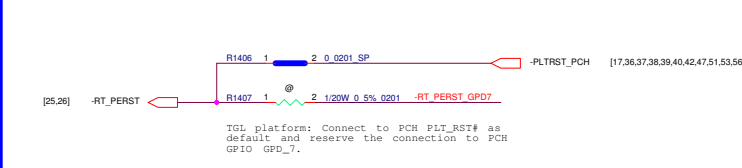
-DRAMRST PU



PCH PD for Glitch Free



TBT Re-timer PERST



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PCH PCIE/USB2&3/SPI/MISC



PCIE Port Assignment

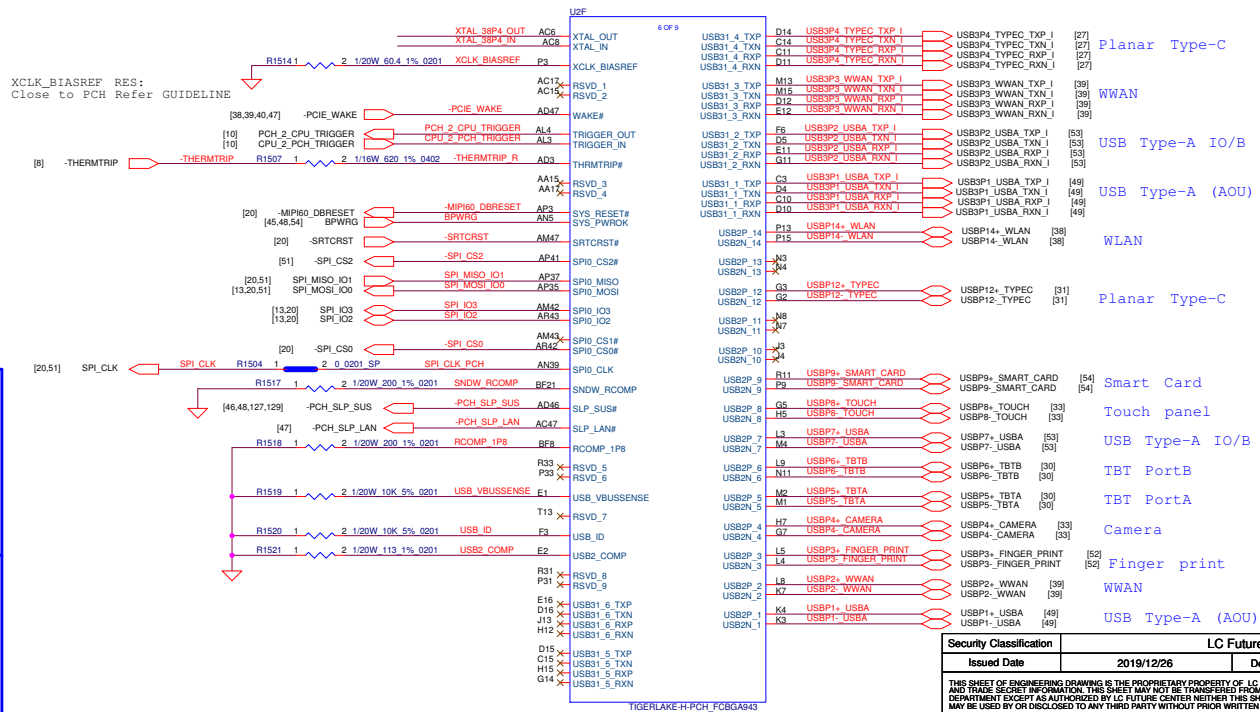
Port Number	Function
Port 5	GbE
Port 6	WLAN
Port 7	WWAN
Port 8	SD Card
Port 9~12	M.2 SSD1
Port 17~20	M.2 SSD2

USB3 Port Assignment

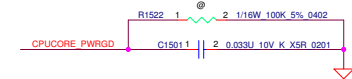
Port Number	Function
Port 1	USB Type-A (AOU)
Port 2	USB Type-A IO/B
Port 3	WWAN
Port 4	Planar Type-C

USB2 Port Assignment

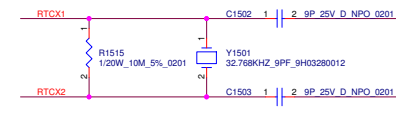
Port Number	Function
Port 1	USB Type-A (ACU)
Port 2	WWAN
Port 3	Fingerprint
Port 4	Camera
Port 5	TBT Port A
Port 6	TBT Port B
Port 7	USB Type-A IO/B
Port 8	Touch Panel
Port 9	Smart Card
Port 12	Planar Type-C
Port 14	Bluetooth



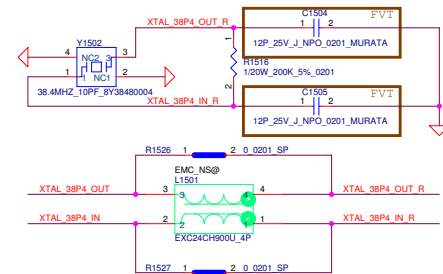
CPUCORE_PWRGD



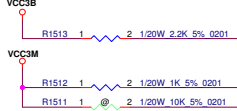
32.768KHz



38.4MHz Crystal




Others PU

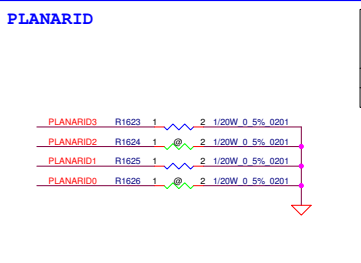
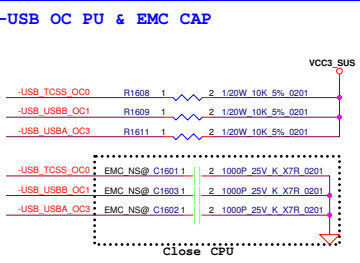
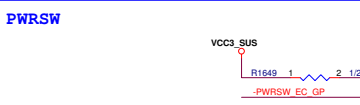
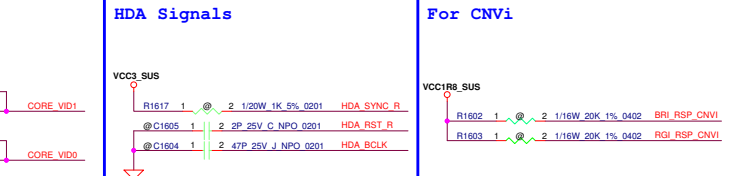
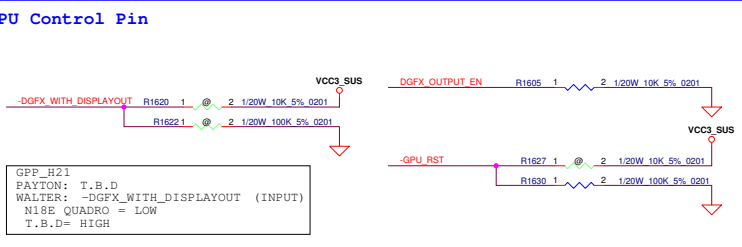
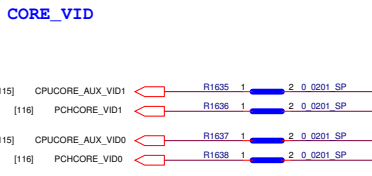
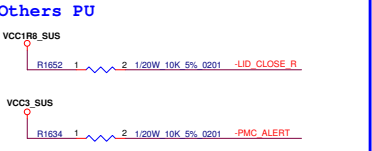
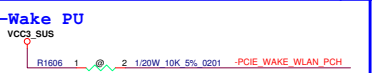
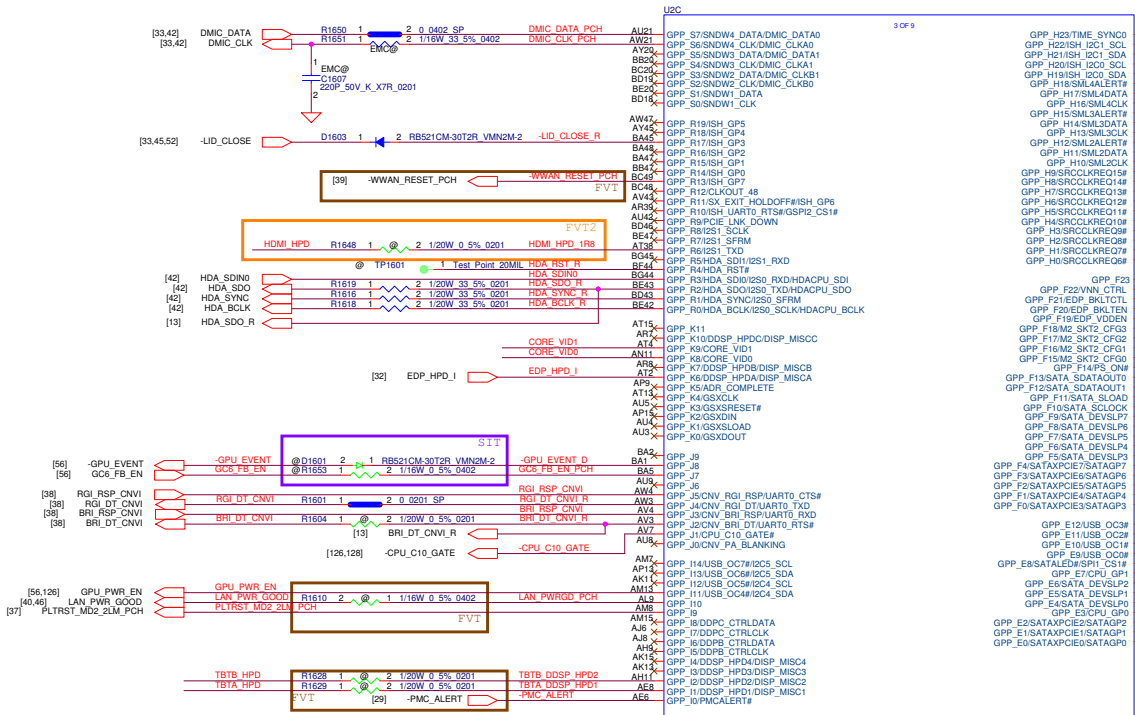


PCH PD for Glitch Free

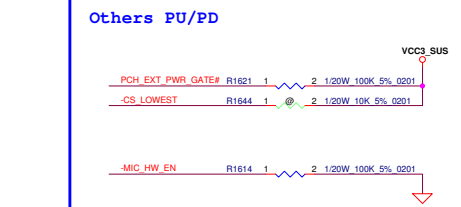
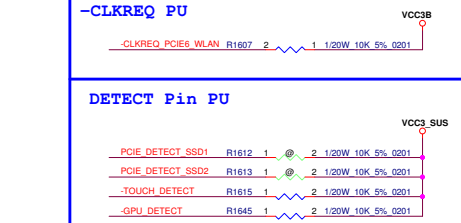
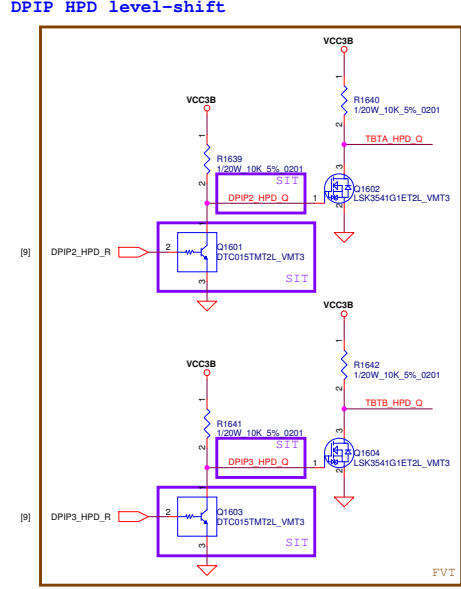


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Size	Document Number	Revision		Rev. 0	
Custom	<p>Exptor & Blackbird Gen2</p>				
Date:	Thursday, Aug 29, 2021	Sheet:	15	of	133

PCH GPIO(1/2)



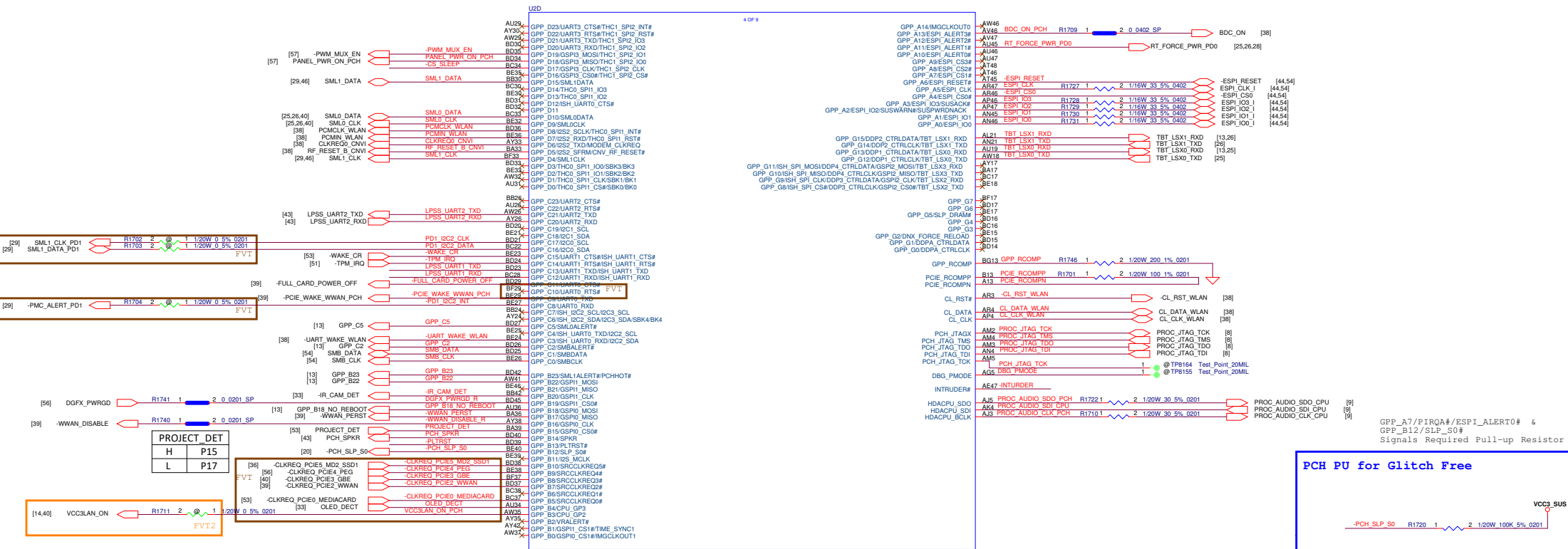
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Issued Date	2019/12/26	Deciphered Date
Deciphered Date	yyyy/mm/dd	
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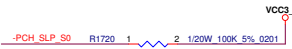
PLANAR ID				
TABLE	3	2	1	0
	R1623	R1624	R1625	R1626
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

LEVEL	PLANARID[3..0]	CPU	PCH
PDV		-----	-----
EVT	0001b	ES1	ES1
FVT	0010b	ES2	ES1
FVT2	0011b	ES2	ES1
SIT	0100b	QS	QS
SVT	0101b	MP	MP

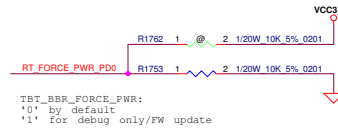
PCH GPIO(2/2)



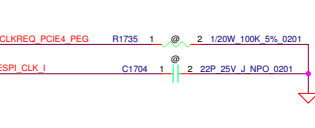
PCH PU for Glitch Free



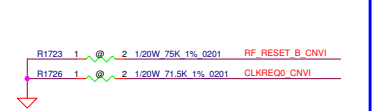
TBT BBR_FORCE_PWR



Others PD



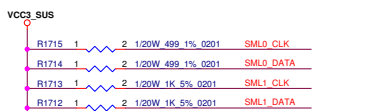
For CNVI



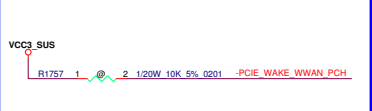
-CLKREQ PU



SMBus PU



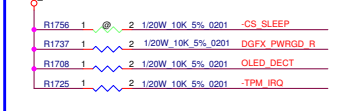
-Wake PU



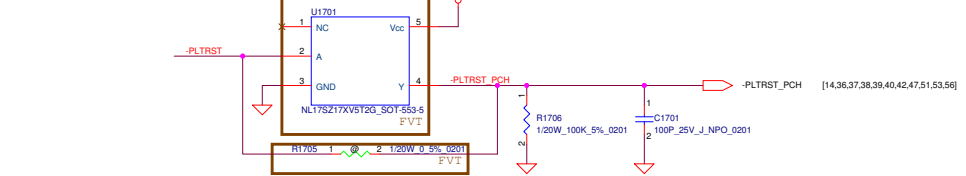
UART PU



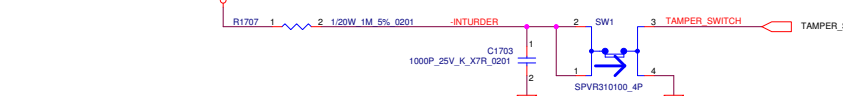
Others PU



PLTRST BUFF



INTRUDE



DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE)

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PCH POWER

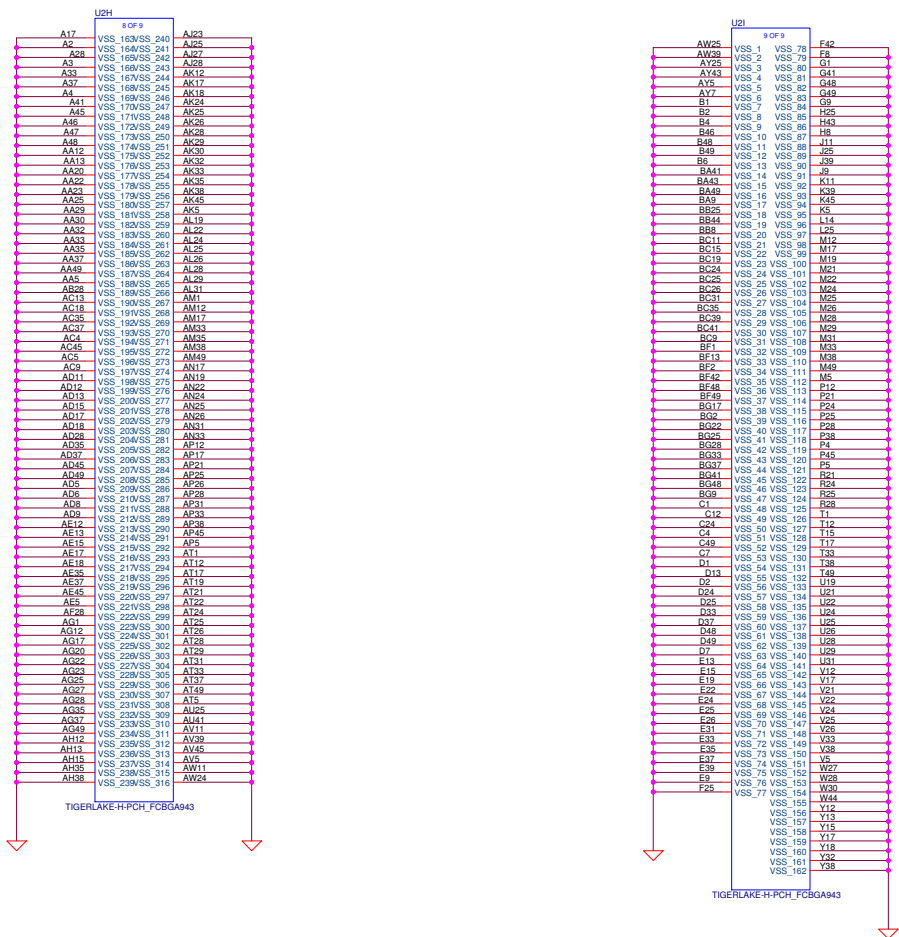
This schematic diagram illustrates the power distribution network for the PCH (Platform Controller Hub) section of a system. It shows various voltage rails such as VCCVCC, VCCPRIM_3P3, VCCIRB_OUT_FET, VCCPRIM_IR05, VCCIRB_SUS, VCCPRIM_IP8, VCCA_CLKLDO_IP8, VCCSM, and VCCPSW_3P3. The circuit includes numerous resistors (e.g., R1813, R1816, R1826, R1829), capacitors (e.g., C1806, C1807, C1808, C1809, C1802, C1803, C1810-C1813, C1815, C1817, C1818, C1819, C1820), and integrated circuits like U2G and TIGERLAKE-H-PCH_FCBGA943. Current values are specified at several points, including 200mA, 12mA, 1.6A, 5mA, 9.7A, 2.2mA, 3mA, 12mA, and 9mA. Test points TP1801 through TP1803 are also indicated.

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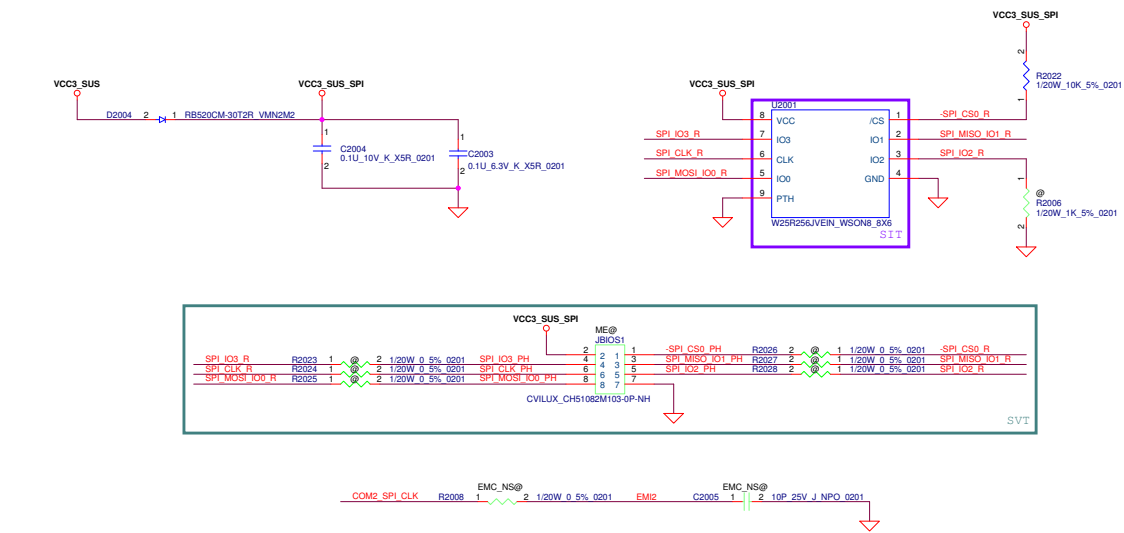
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Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd					PCH TGL-H : POWER
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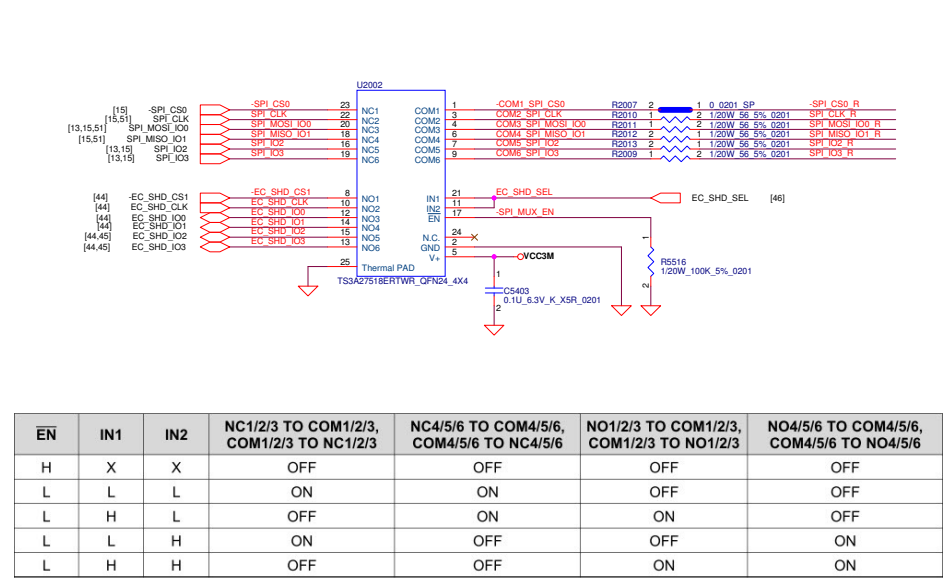
PCH GND



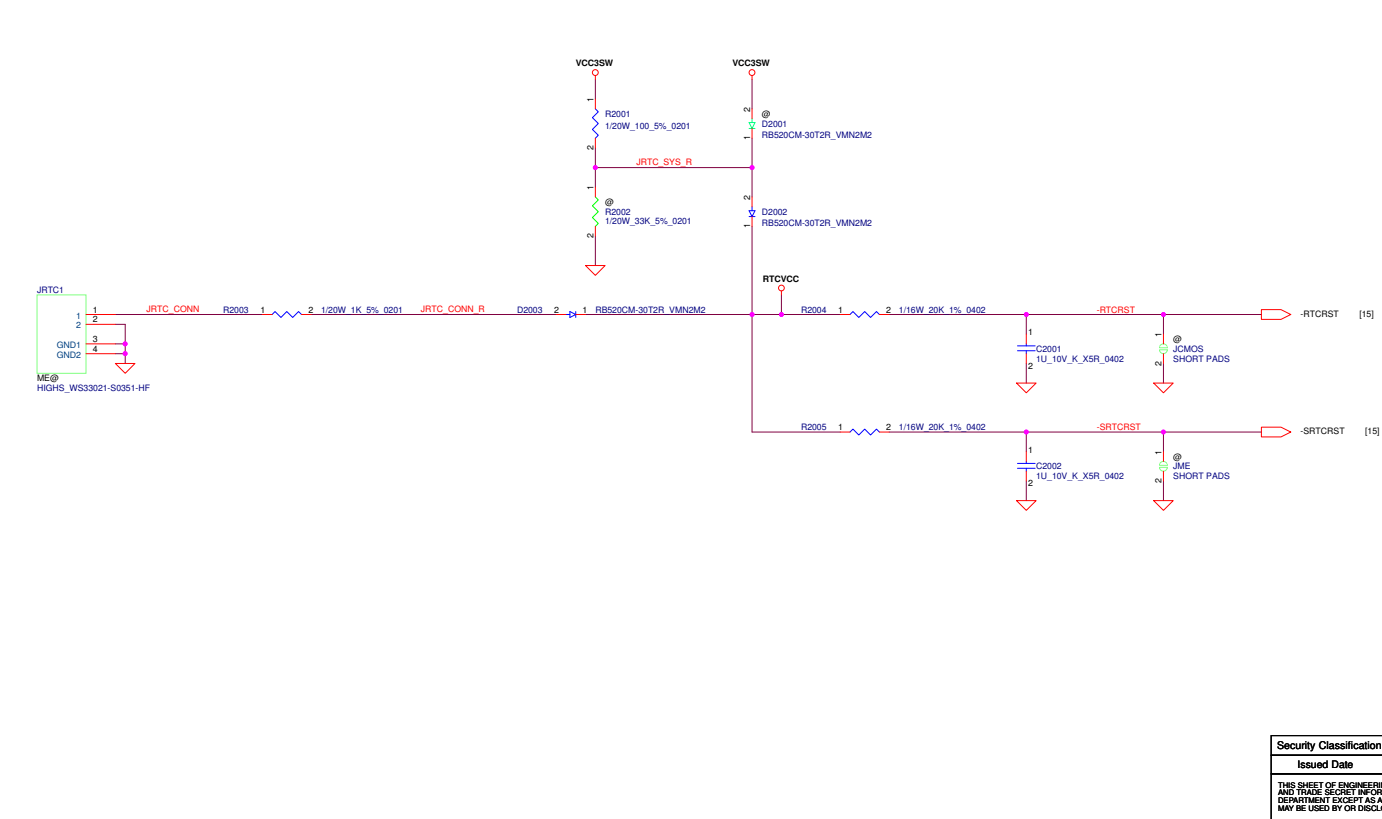
PCH SPI FLASH (Support RPMC)



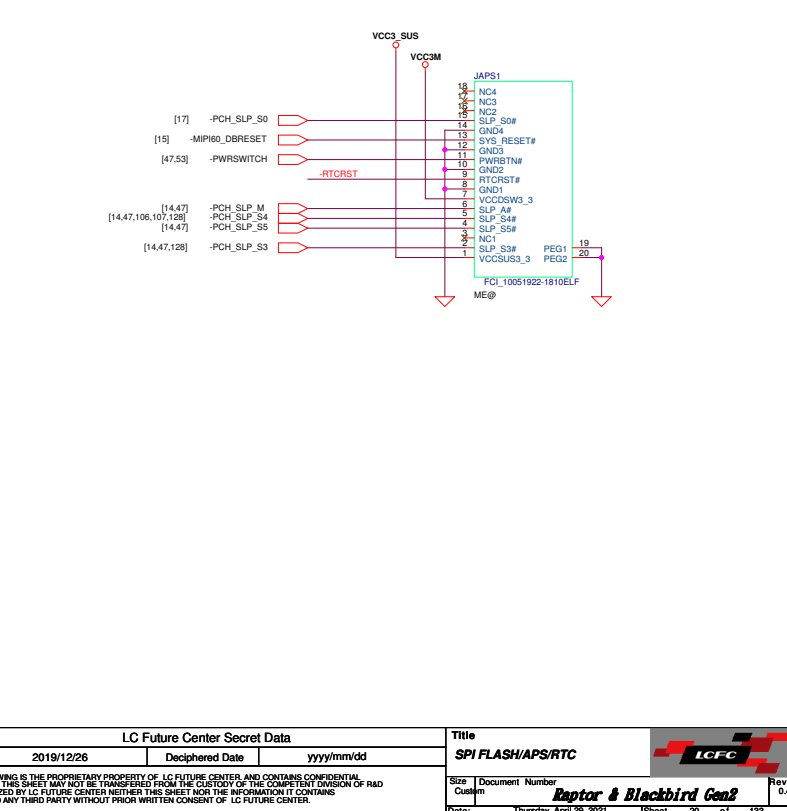
SPI Switch



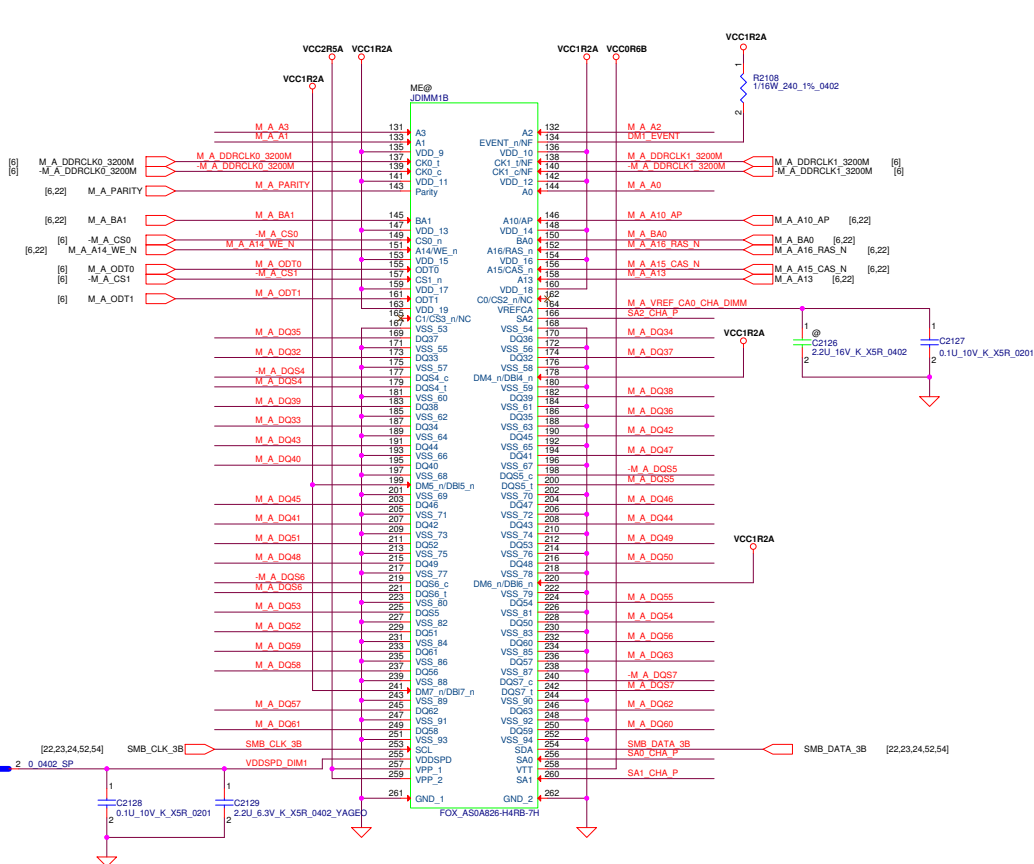
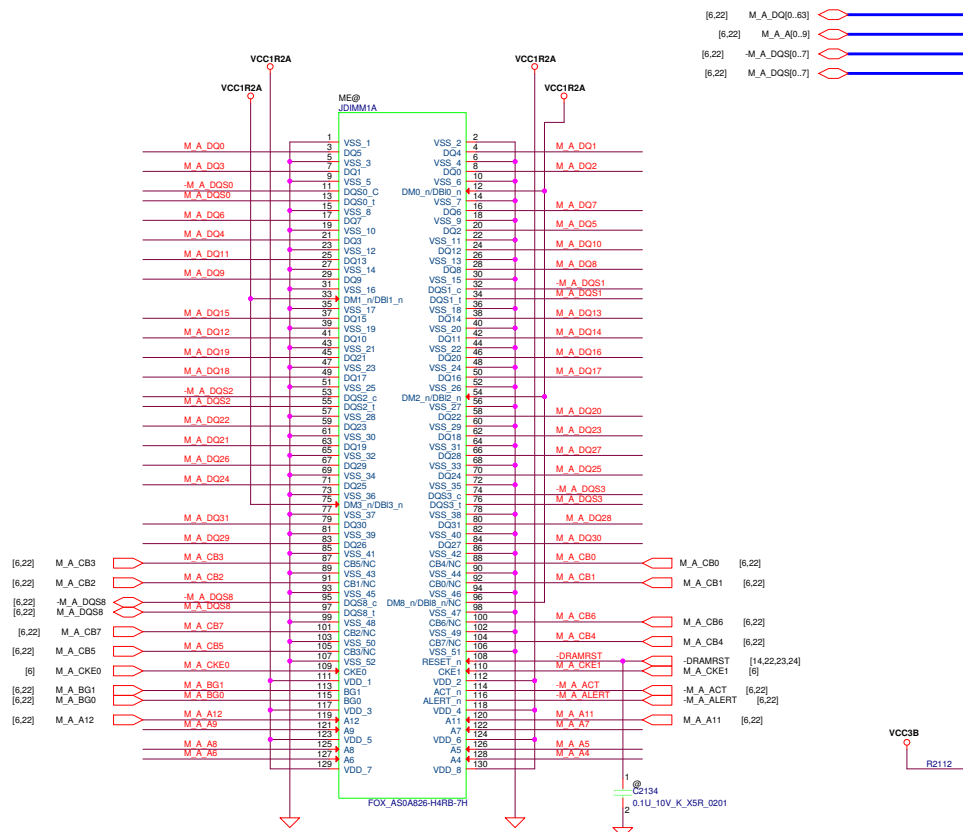
RTC



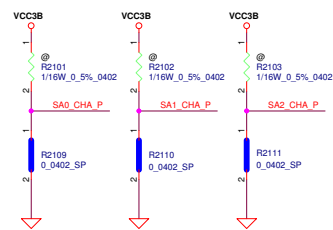
APS CONN



DDR4 CH-A Parimary

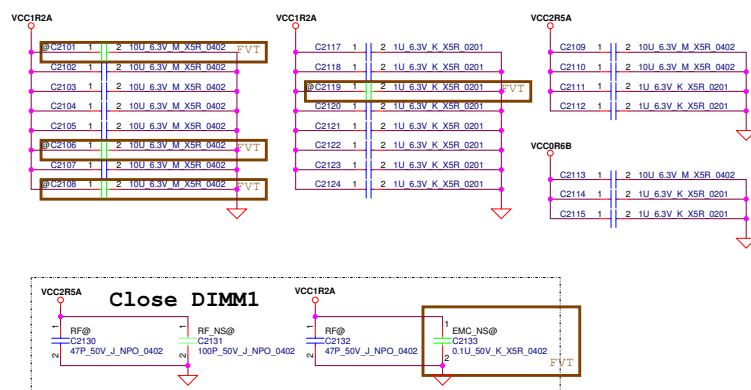


SA0~2

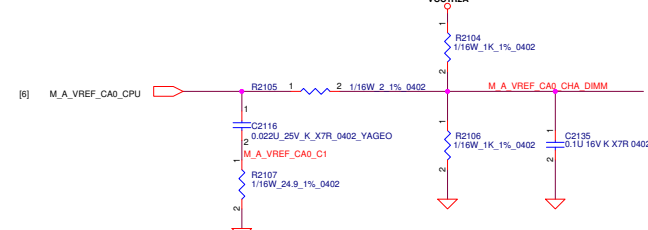



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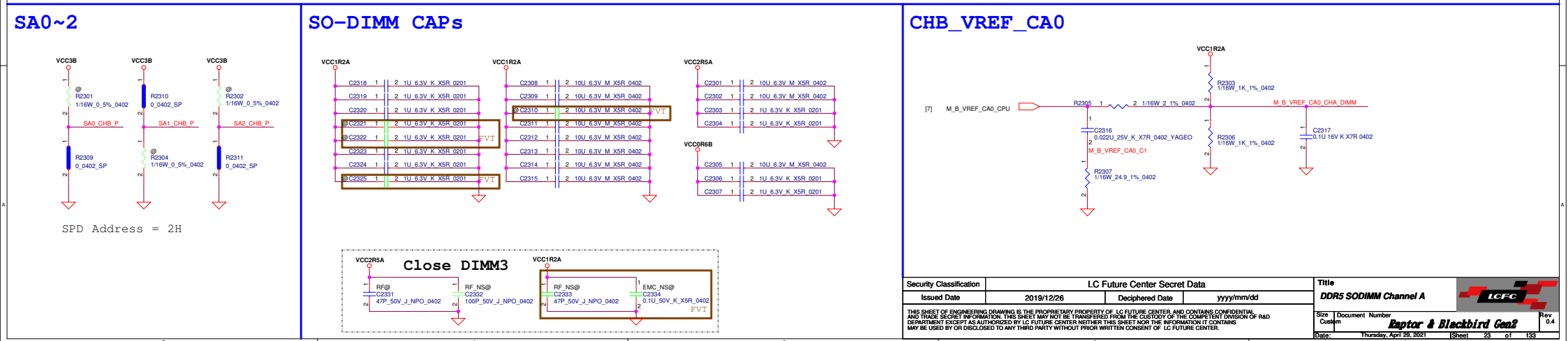
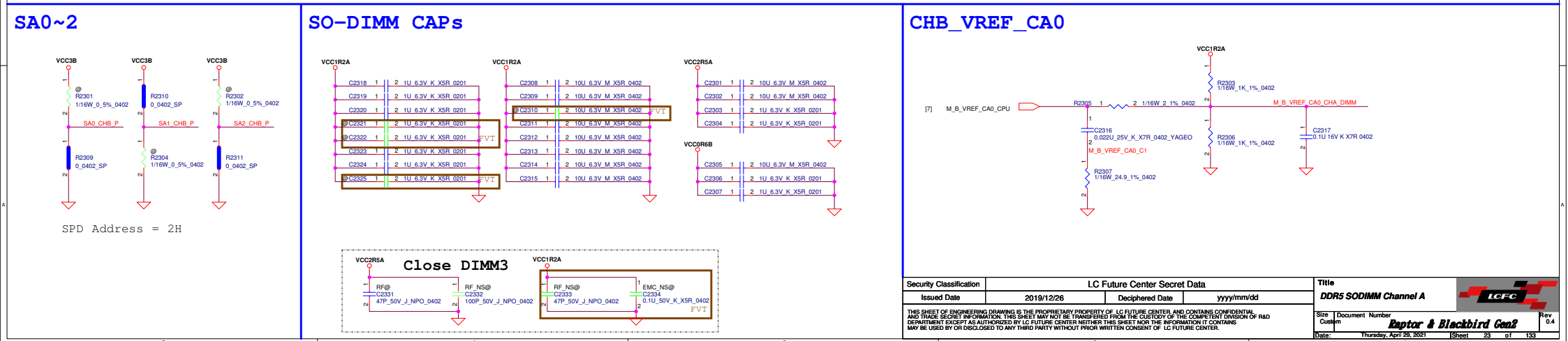
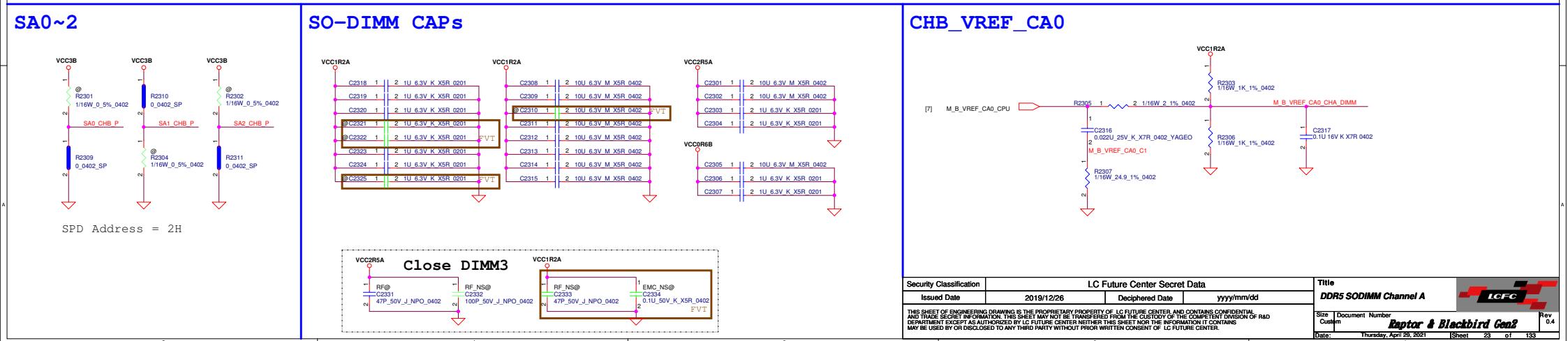
SO-DIMM CAPs



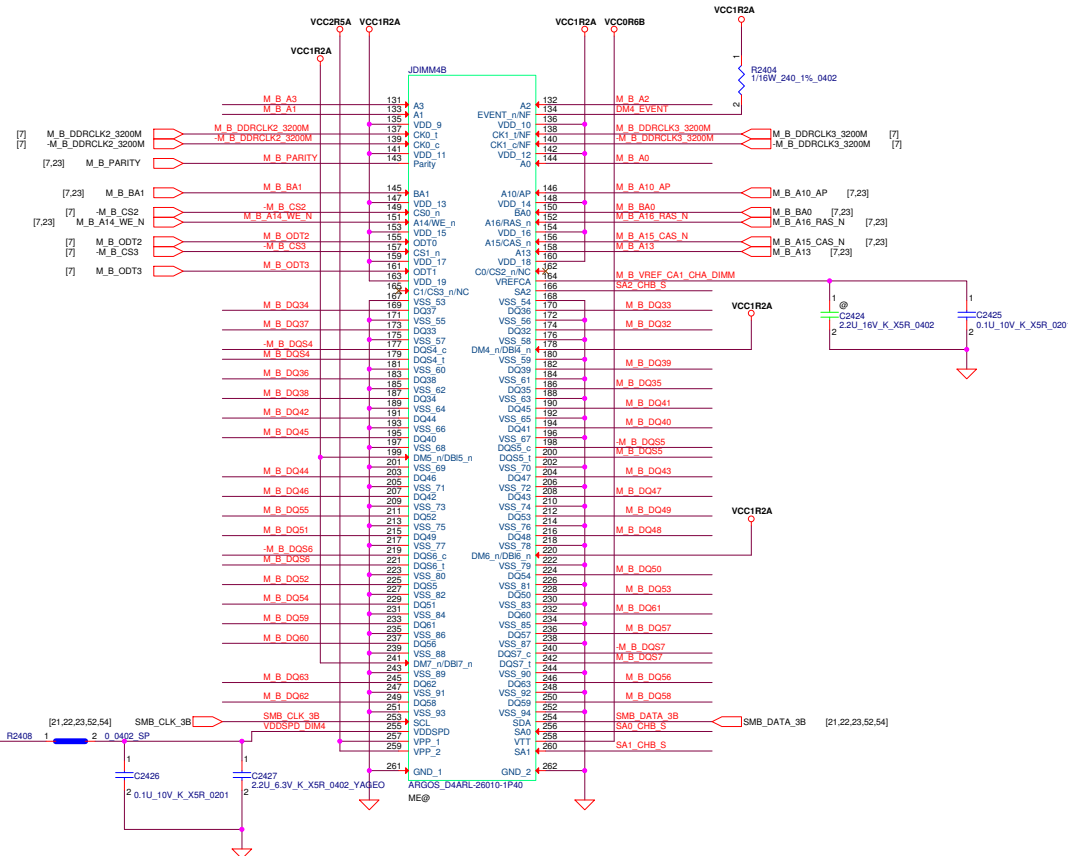
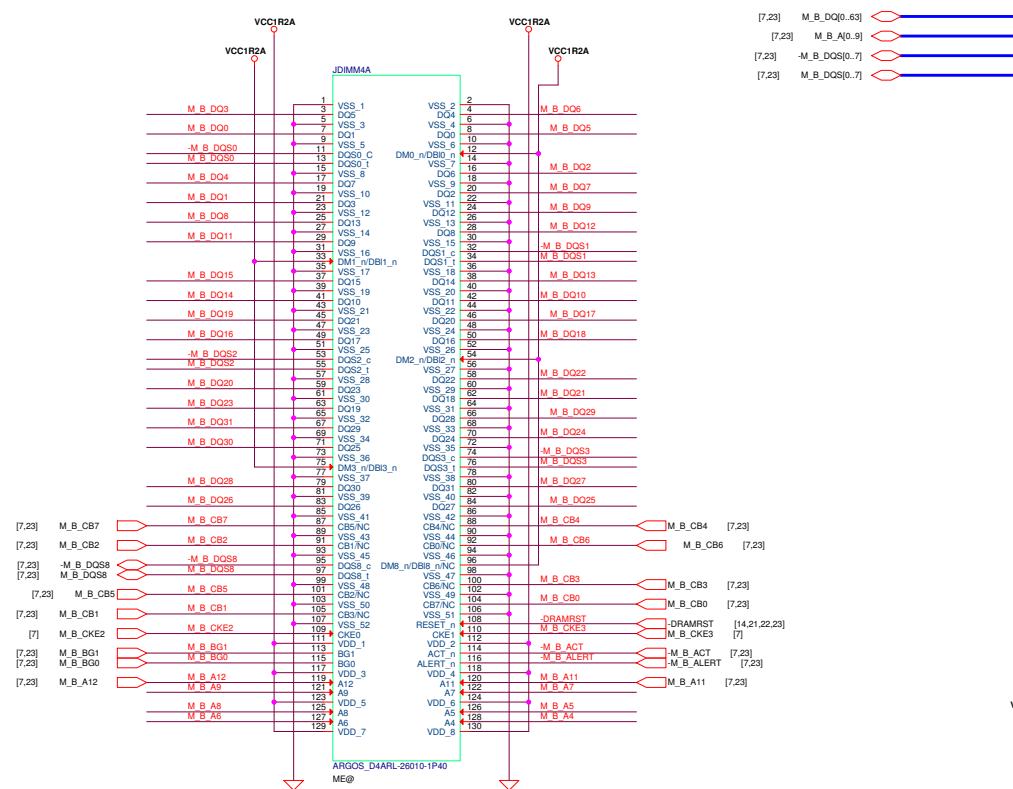
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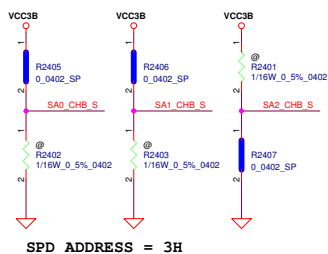
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				<p>Date: Thursday, April 29, 2021</p>		<p>133</p>	
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DDR4 CH-B Secondary

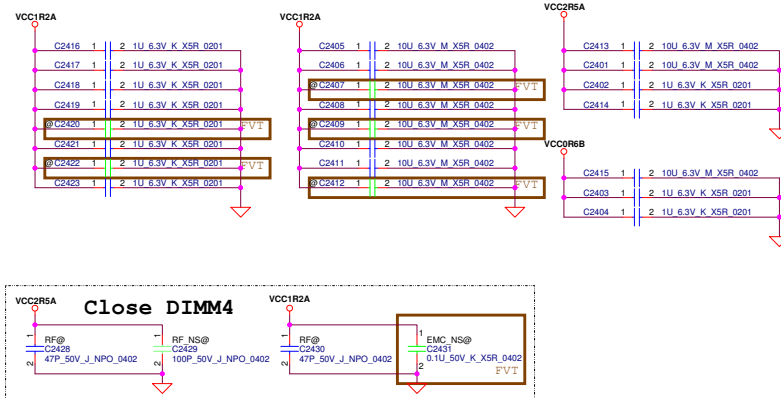


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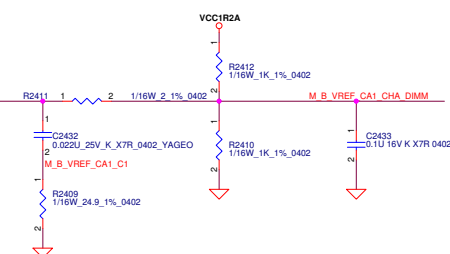



SPD ADDRESS = 3H

SO-DIMM CAPs

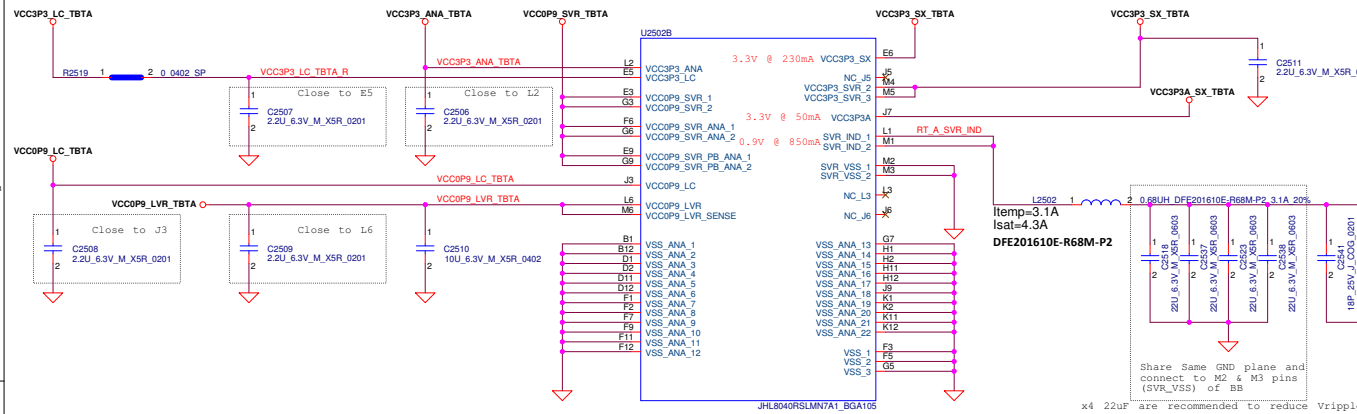
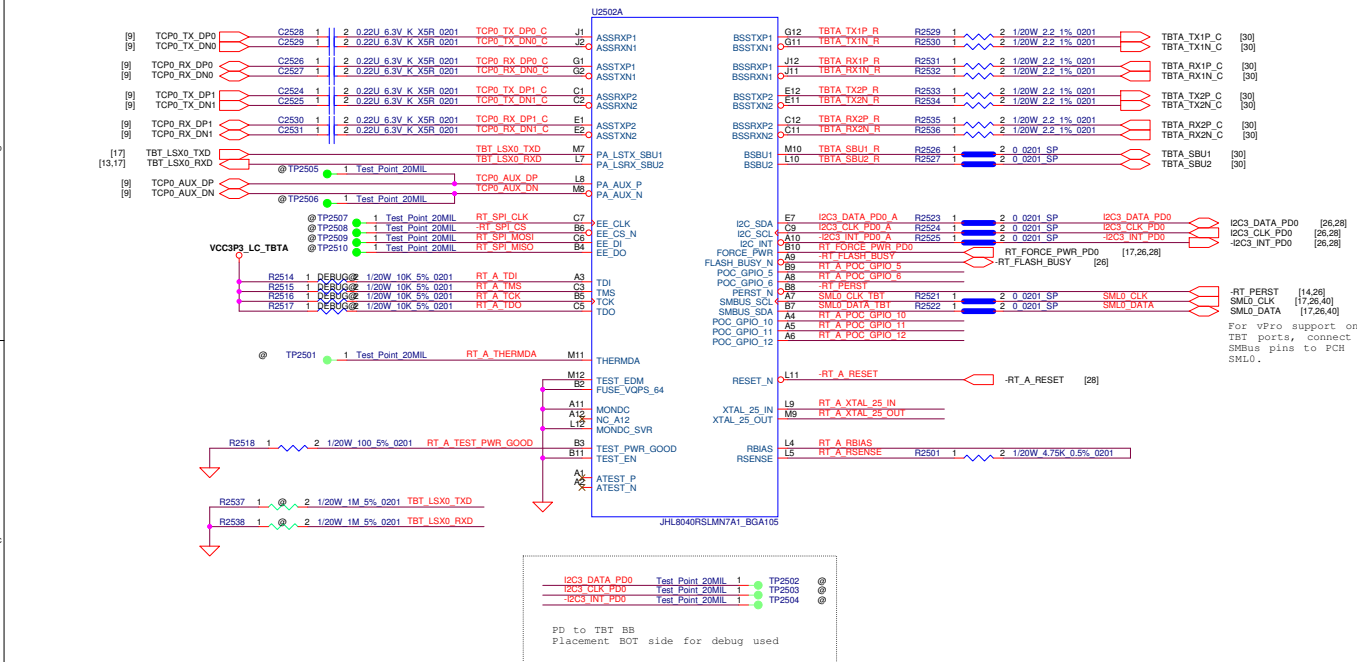


CHB_VREF_CA1



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TBT Re-timer A



TBT Re-timer A Strap pin

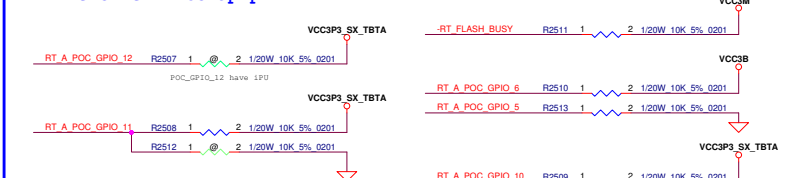


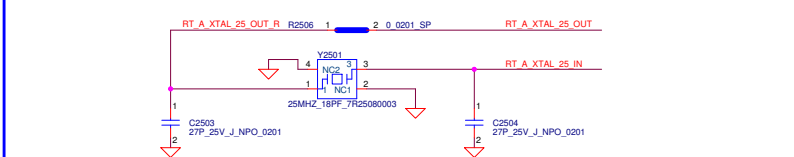
TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

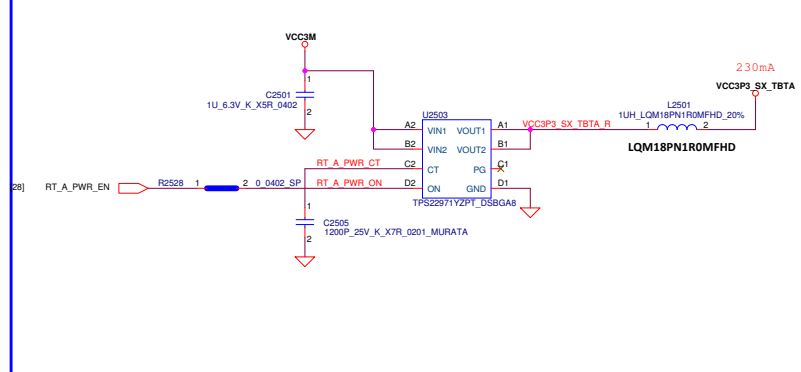
TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

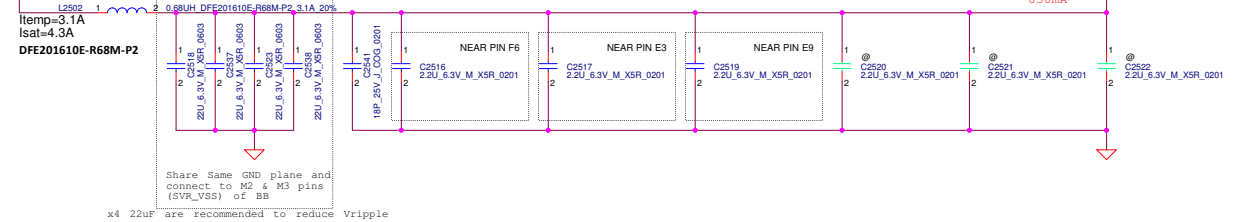
TBT Re-timer A Crystal



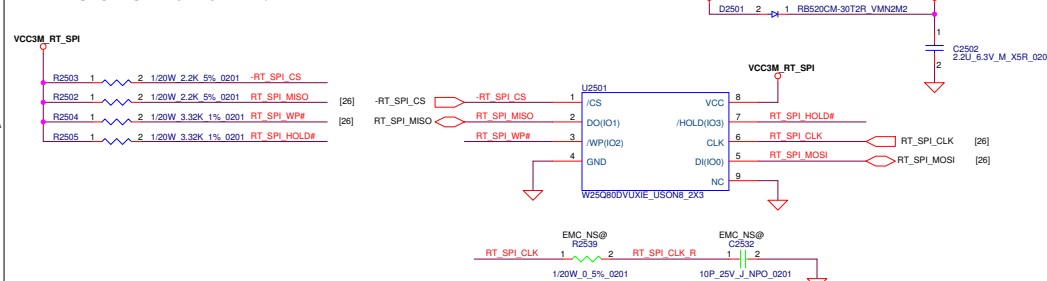
TBTA Power Gate



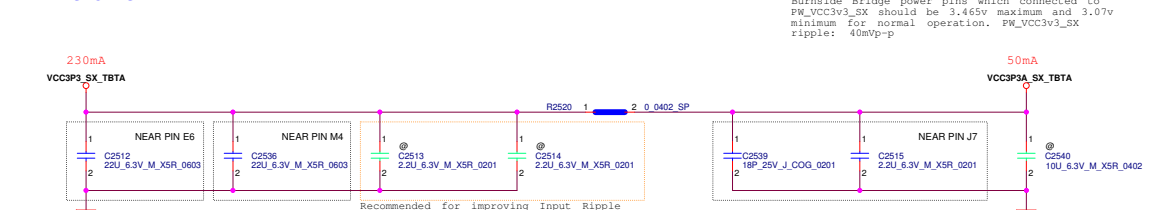
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TBT Re-timer A&B SPI ROM

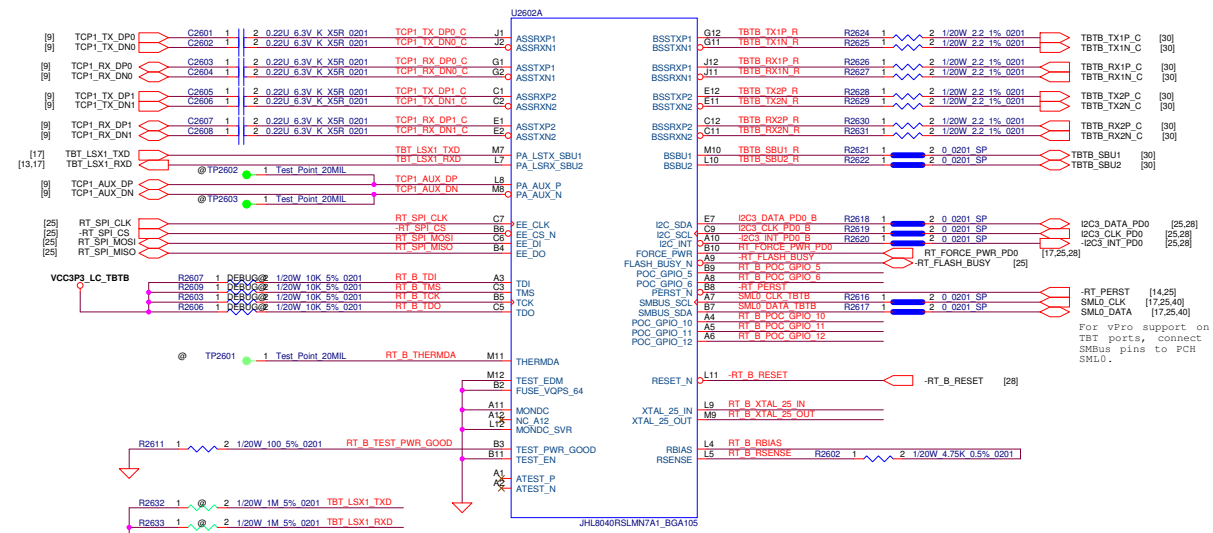


TBT Re-timer A PWR



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Name:		Thursday, April 26, 2021		153	

TBT Re-timer B



TBT Re-timer B Strap pin

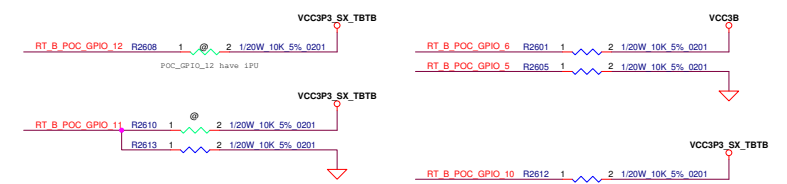


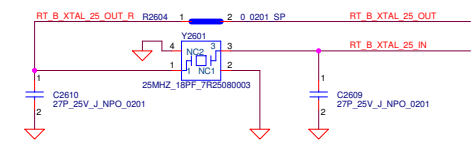
TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

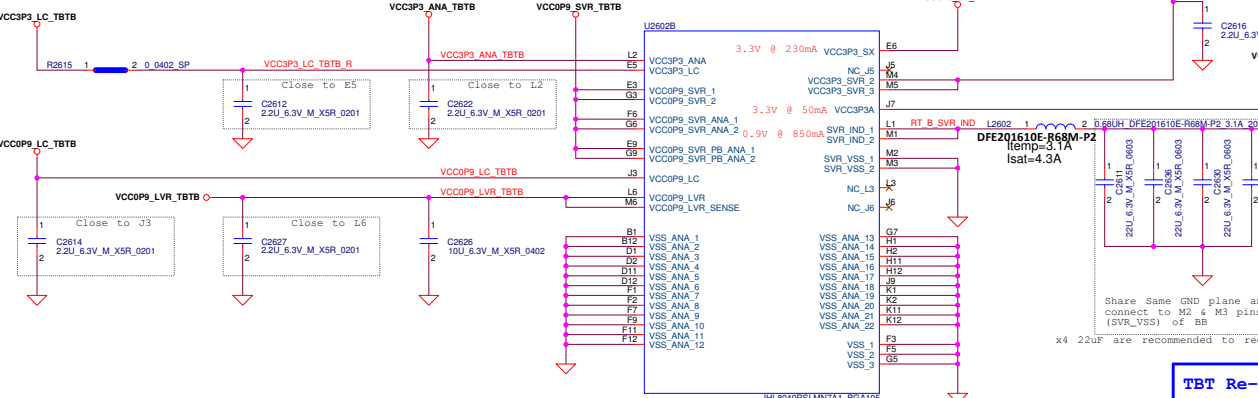
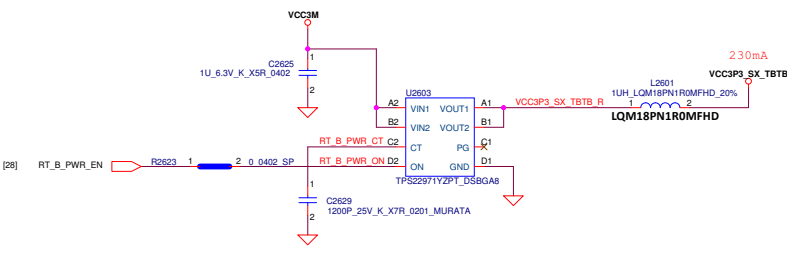
TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

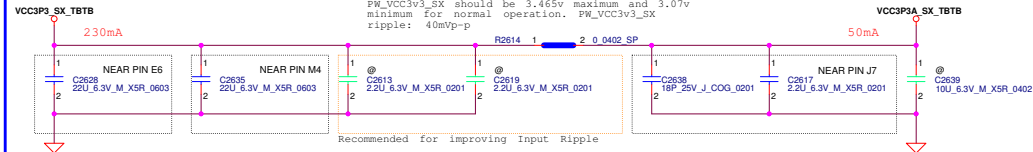
TBT Re-timer B Crystal



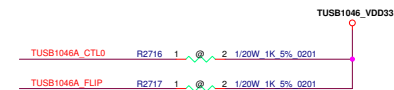
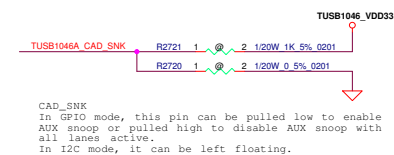
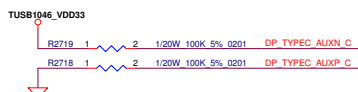
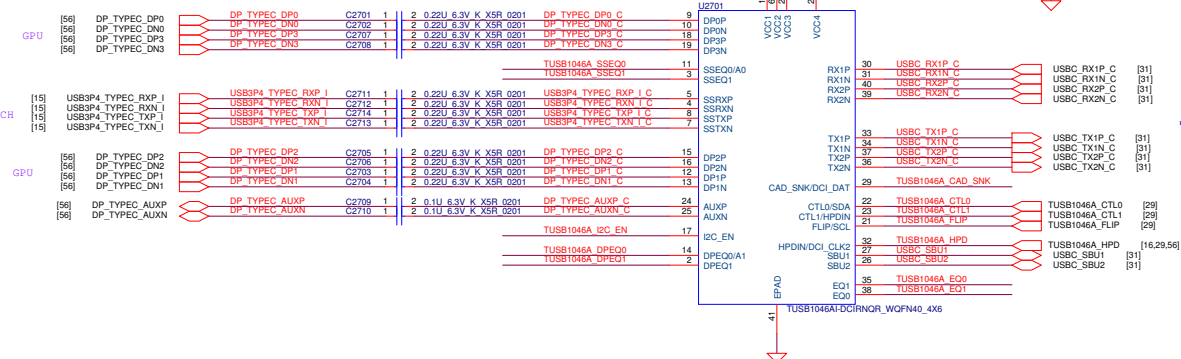
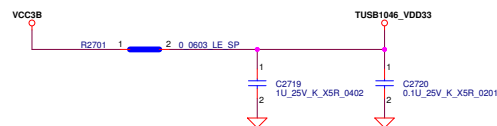
TBTTB Power Gate



TBT Re-timer B PWR

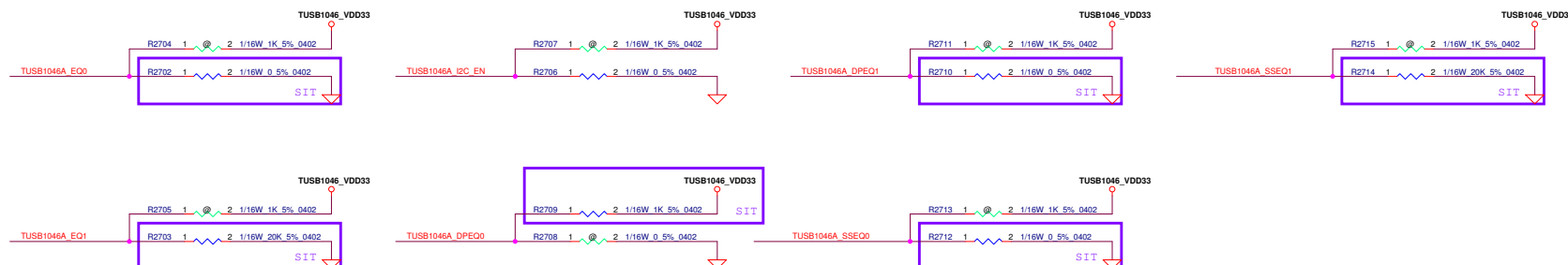



X-Bar TUSB1046A



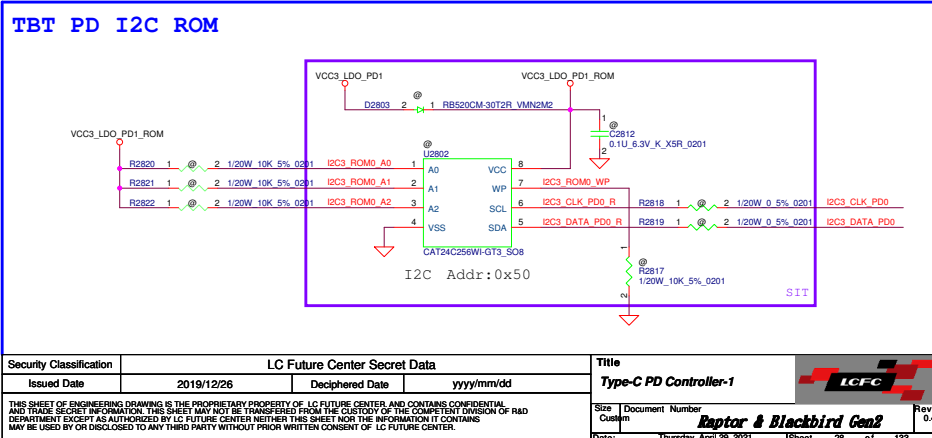
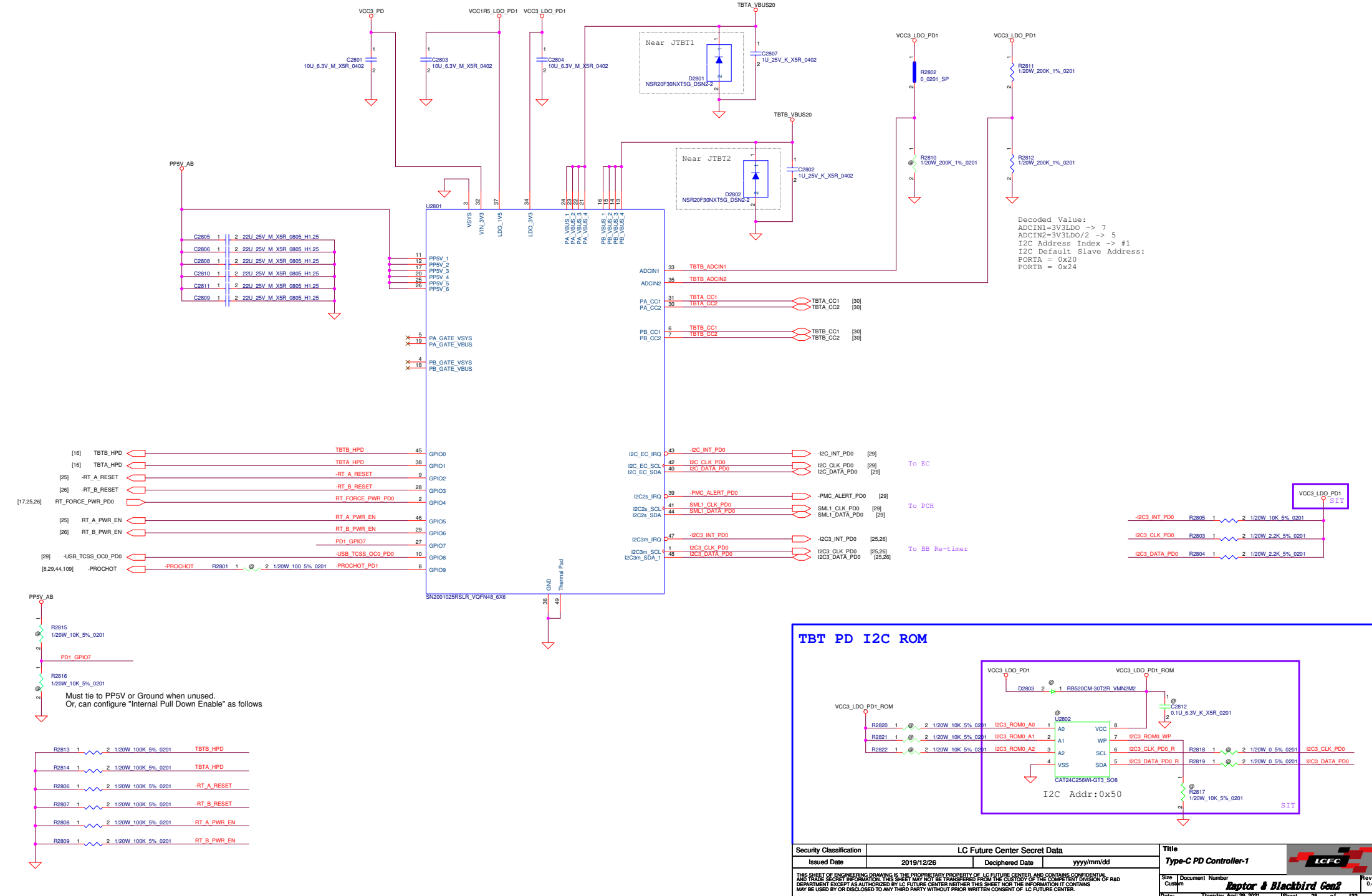
TUSB1046A Strap pin

LEVEL	SETTINGS
0	Option 1: Tie 1K to GND Option 2: Tie directly to GND
R	Tie 20K to GND
F	Float (Leave pin open)
1	Option 1: Tie 1K to VCC Option 2: Tie directly to VCC

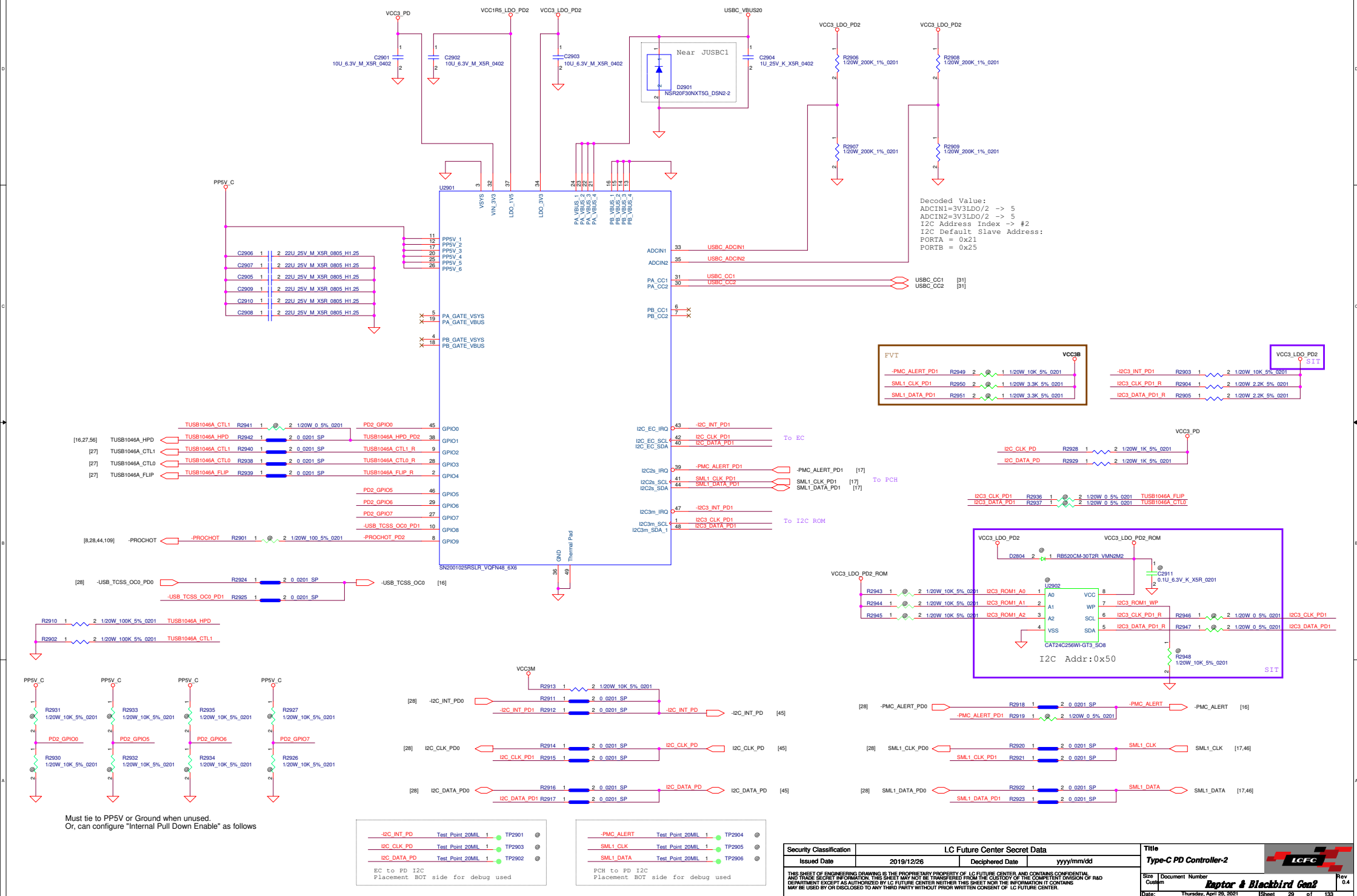


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					Exptor 2	0.4
					Date Thursday, April 26, 2024	Status Blackbox
					27	0.1 133

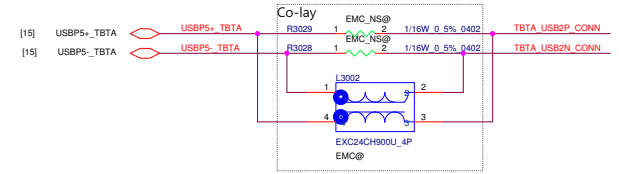
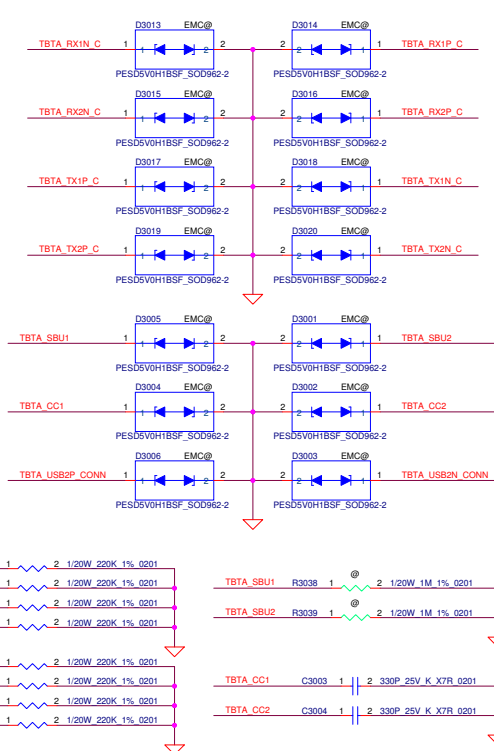
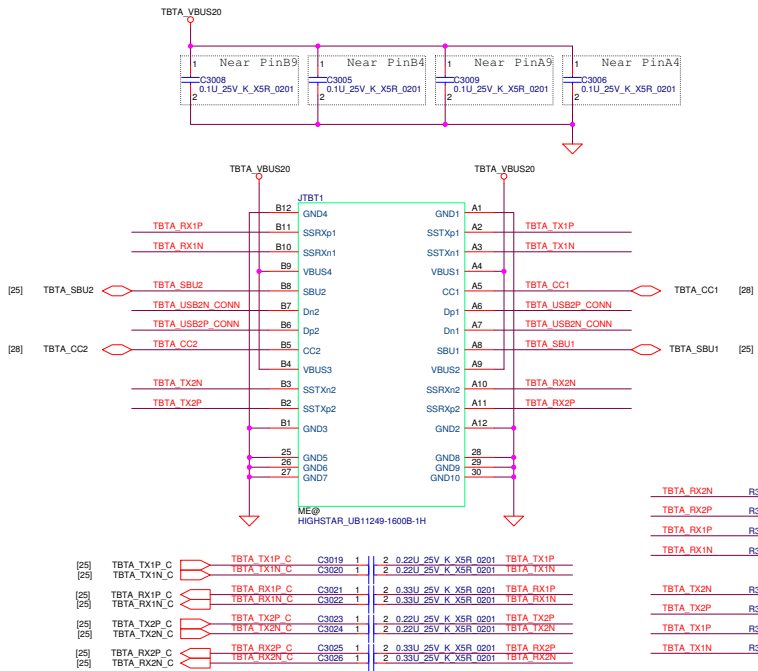
PD Controller-1 TI65994



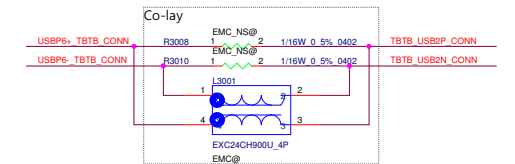
PD Controller-2 TI65994



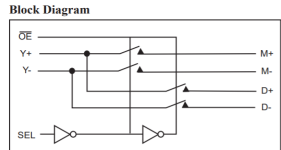
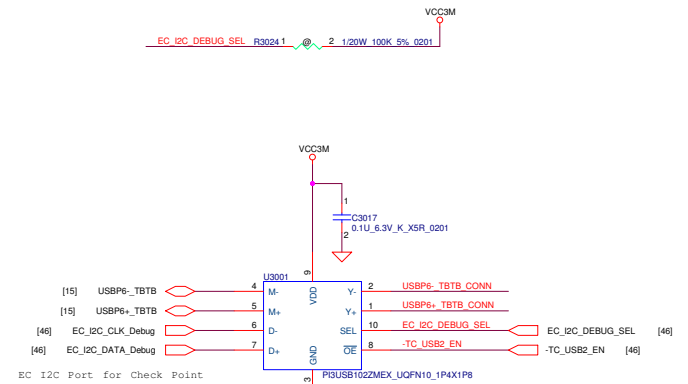
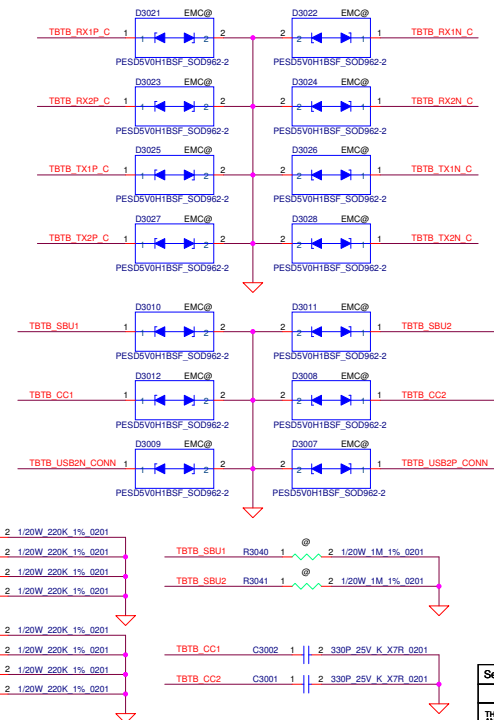
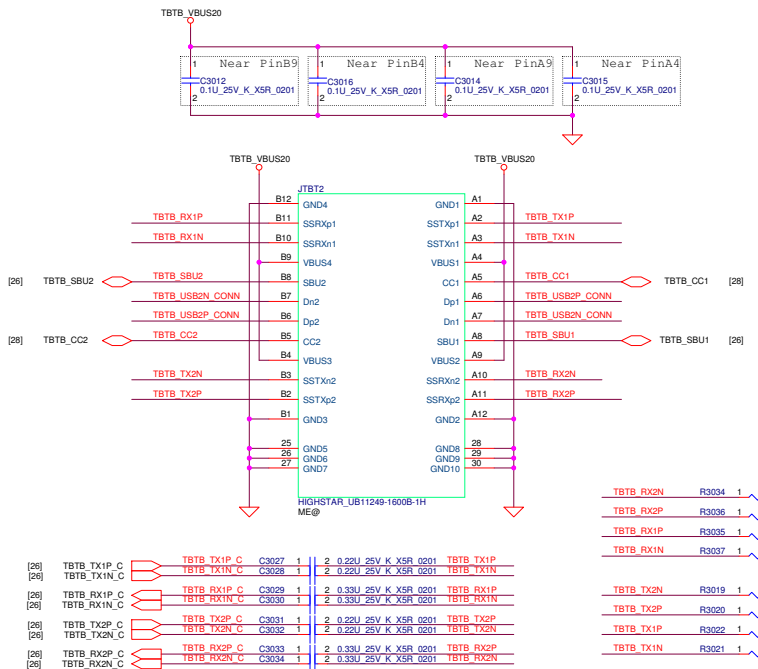
TBT TYPE-C CONN 1



Type-C Debug port (EC I2C Port)




TBT TYPE-C CONN 2

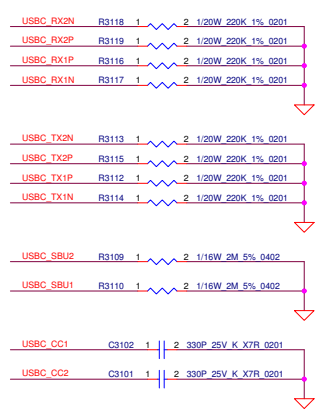
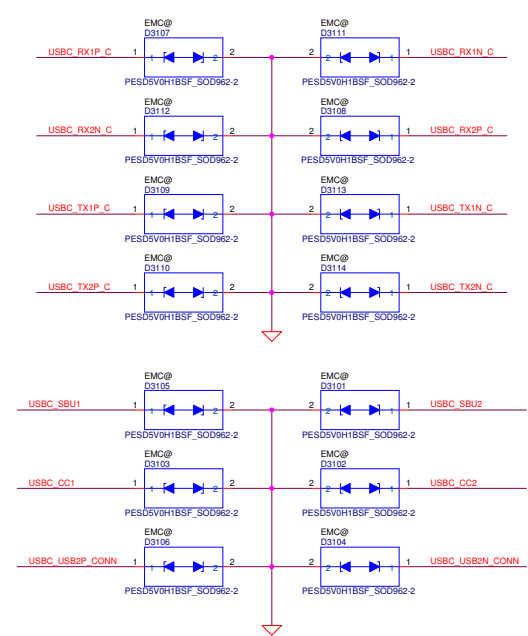
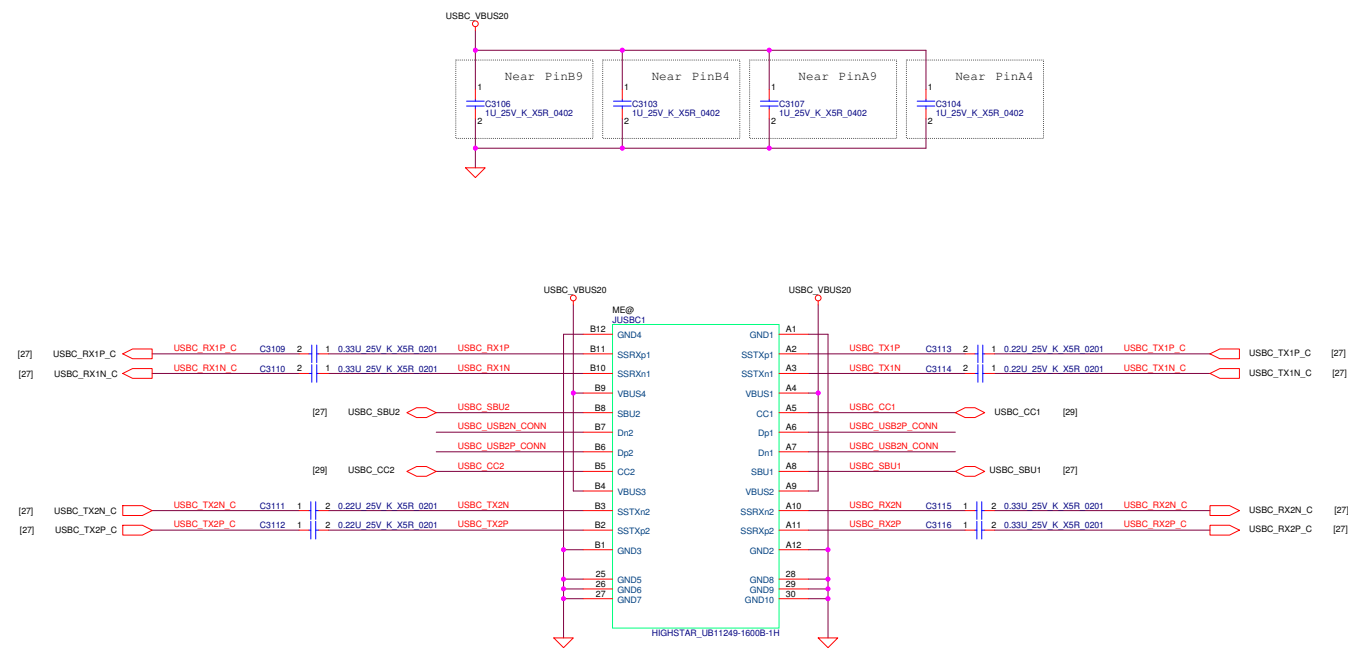


SEL	\overline{OE}	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

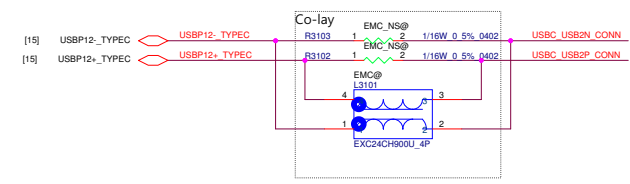
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Size Custom	Document Number	Raptor & Blackbird Gen2			Rev	0.3
Date:	Tuesday, April 29, 2020	Sheet	30	of	133	

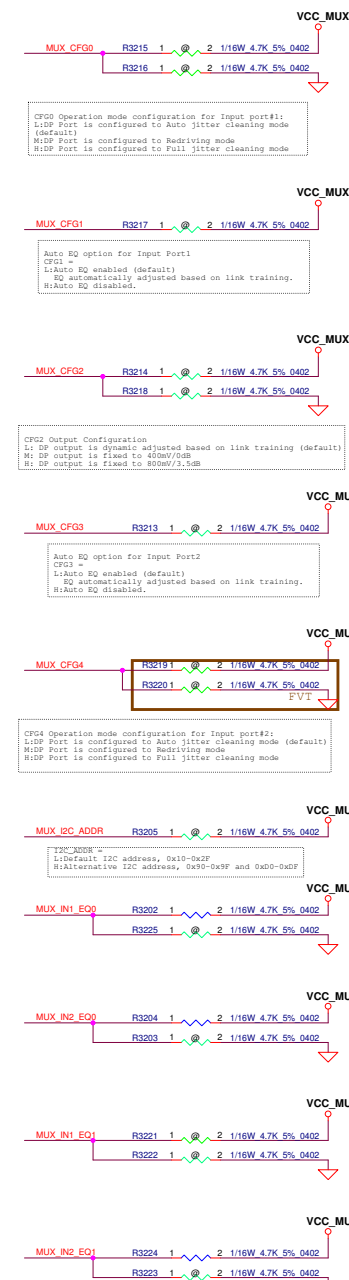
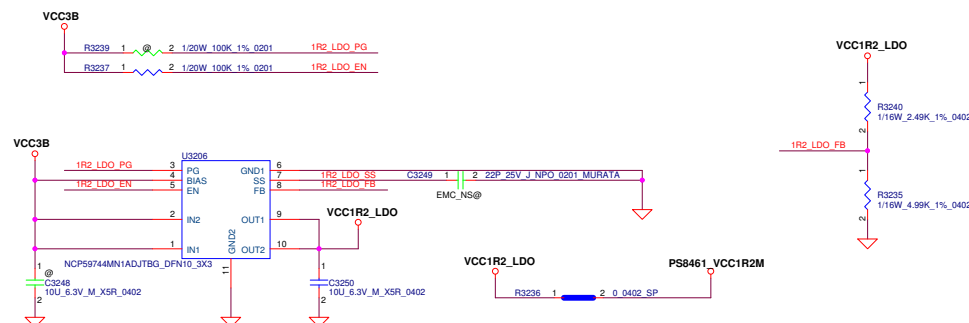
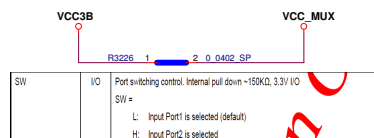
USB TYPE-C CONN 3



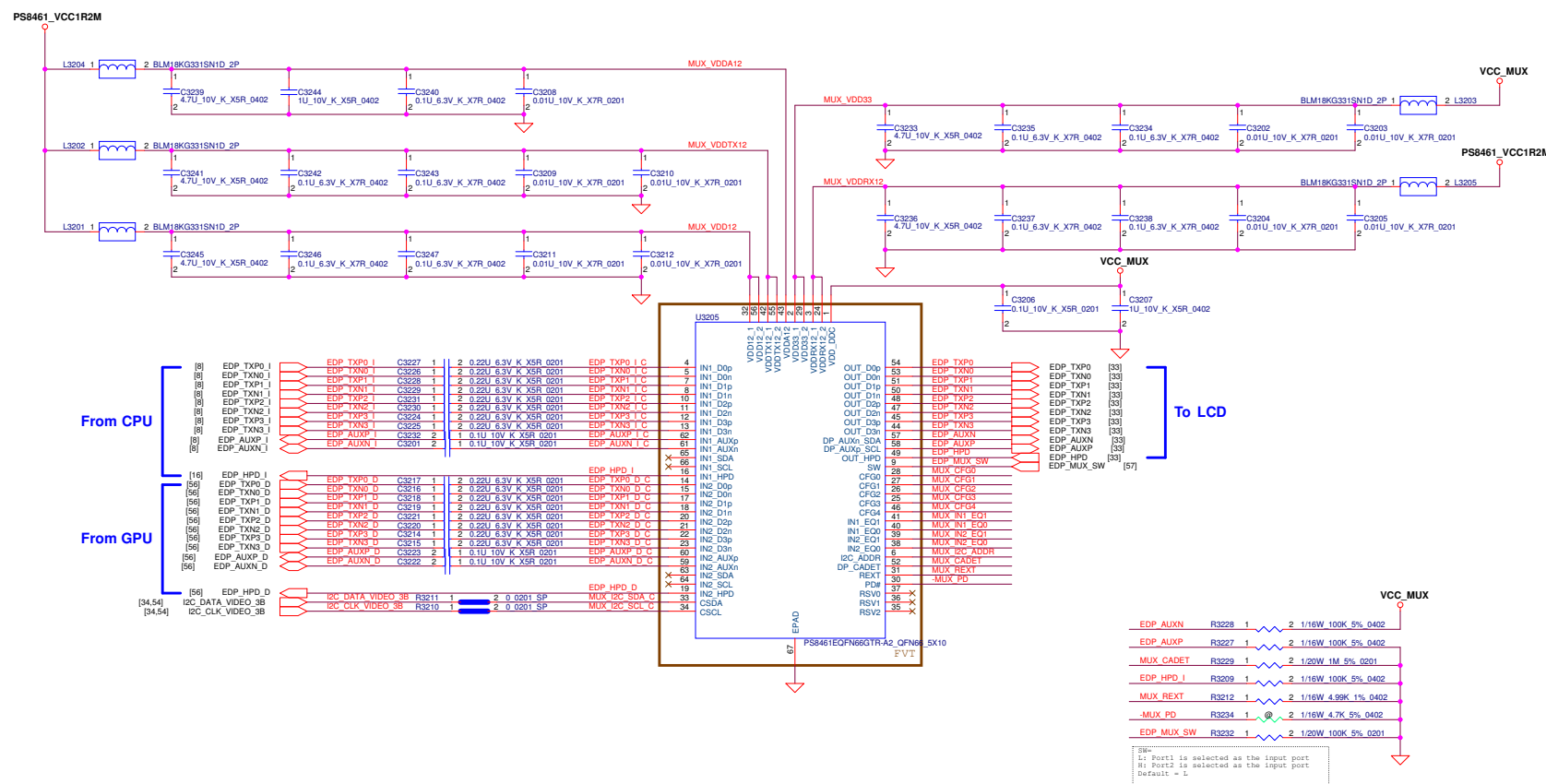
USB2 for TYPE-C CONN 3



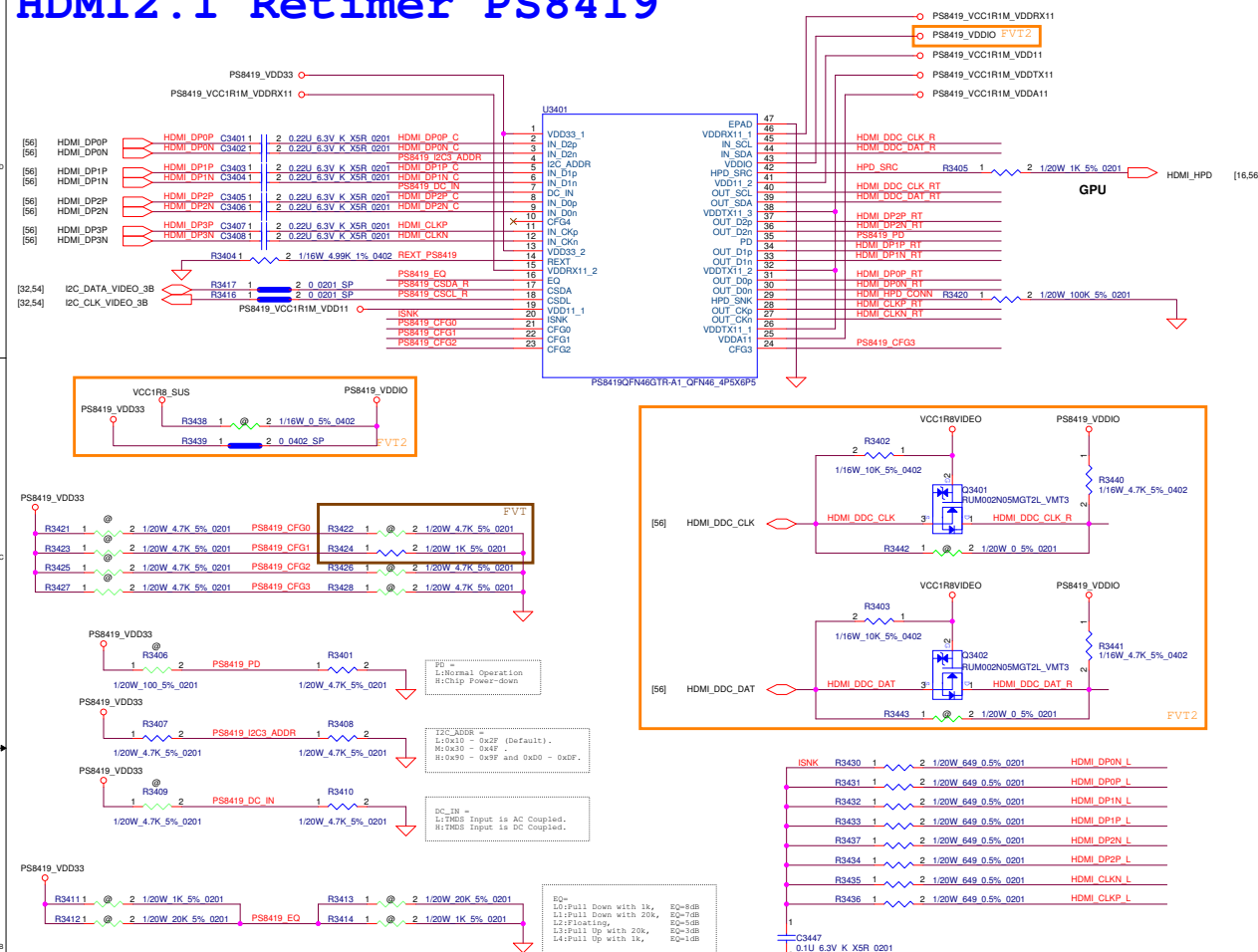
PS8461 Strap pin



eDP Re-driver PS8461

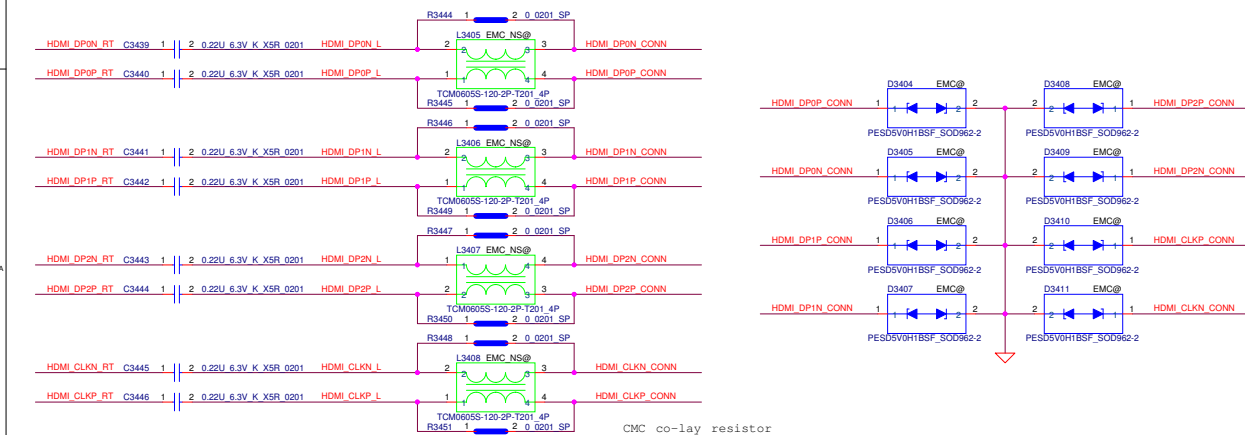


HDMI2.1 Retimer PS8419

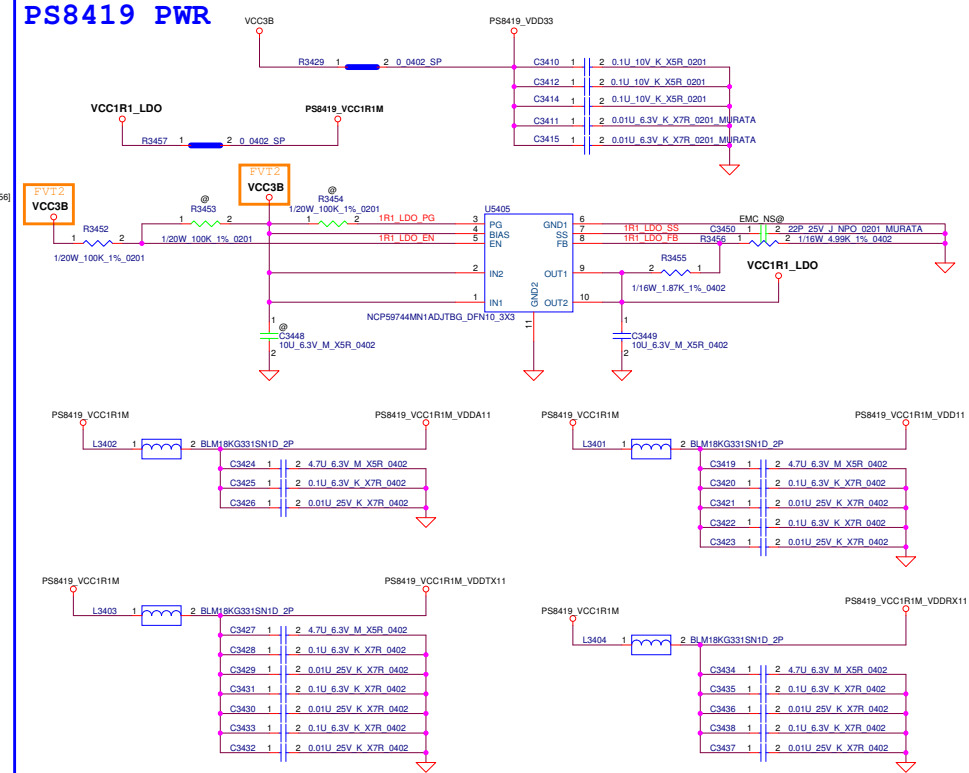


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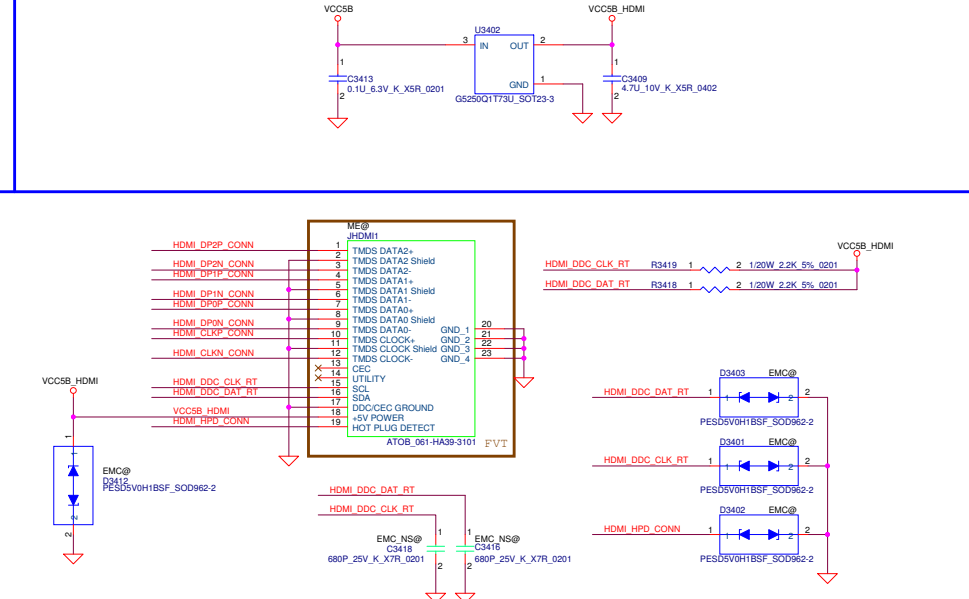
HDMI 2.1 CONN




PS8419 PWR




HDMI CONN PWR

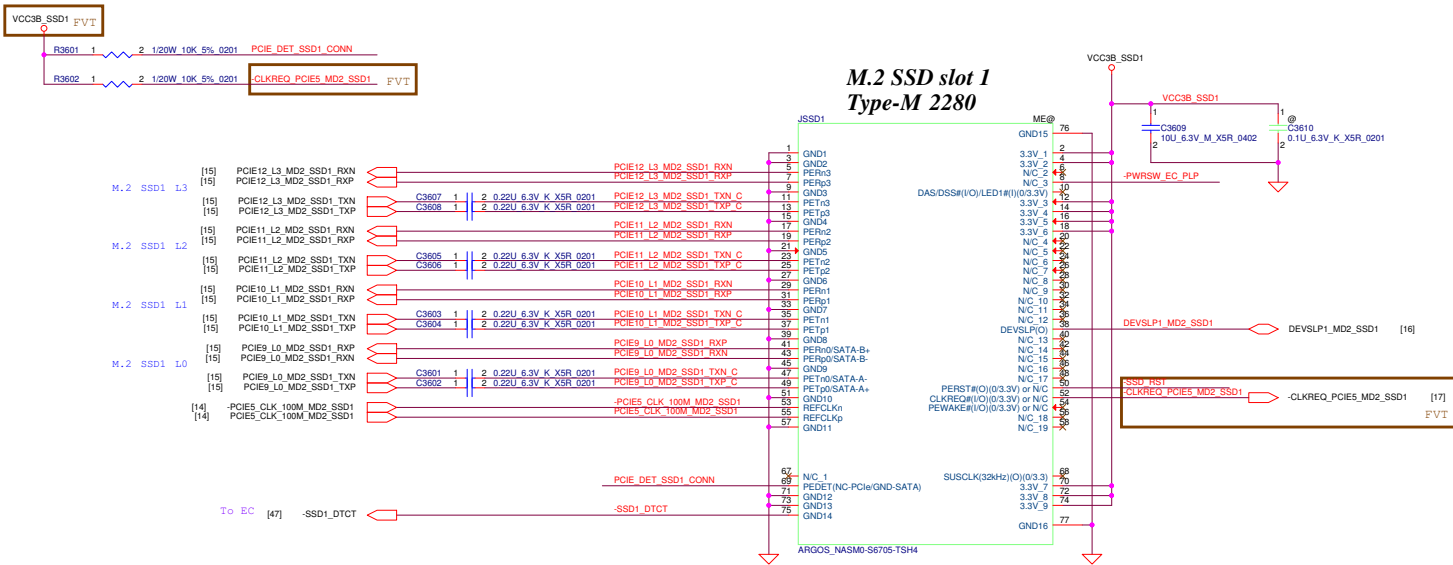


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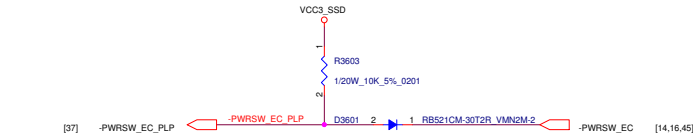
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Issued Date		Deciphered Date		BLANK							
2015/07/16		2016/01/16									
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						<small>Custom</small>					
<small>Date:</small>						<small>Thursday, April 25, 2021</small>		<small>Sheet</small>	<small>35</small>	<small>of</small>	<small>133</small>

M.2 SSD Slot1



SSD Slot1 PWR

PLN for NVMe SSD



SATA/PCIE PEDET

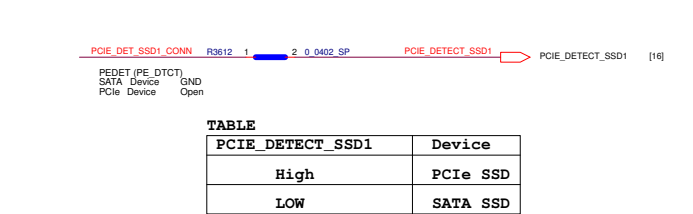
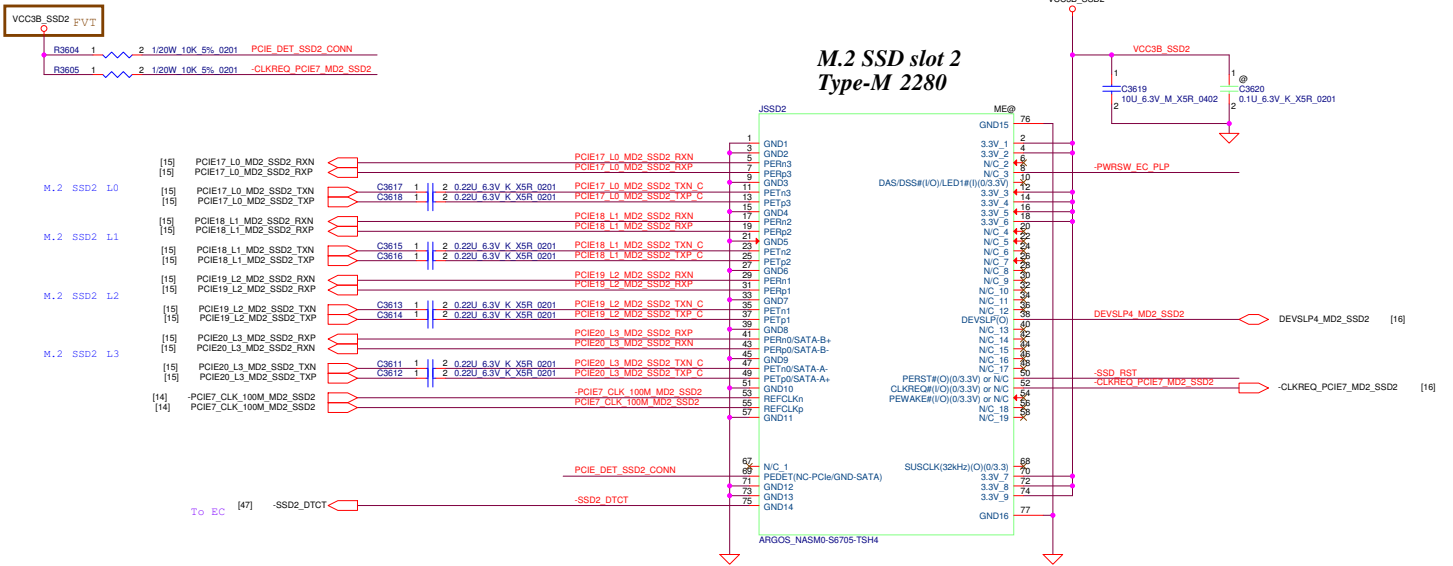
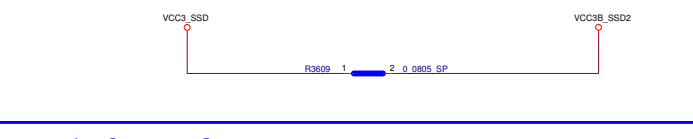


TABLE	
PCIE_DETECT_SSD1	Device
High	PCIe SSD
Low	SATA SSD

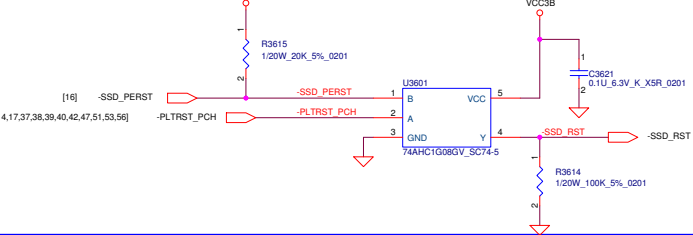
M.2 SSD Slot2



SSD Slot2 PWR



SSD1&2 RTD3



SATA/PCIE PEDET

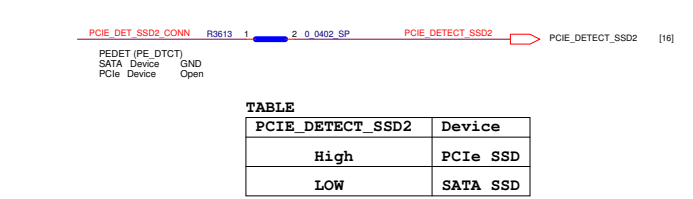
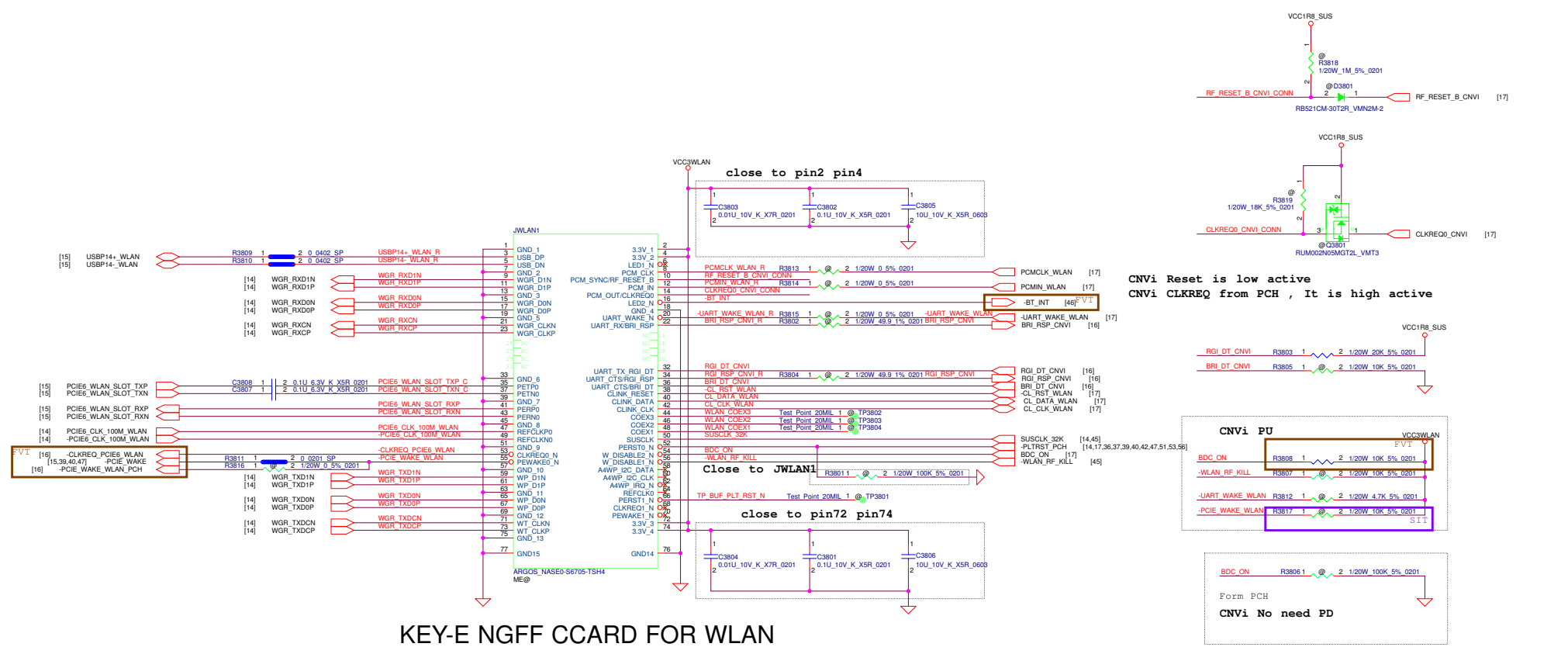
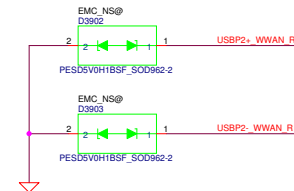
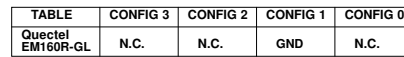


TABLE	
PCIE_DETECT_SSD2	Device
High	PCIe SSD
Low	SATA SSD

WLAN Typhoon peak 2



H=2.00mm Connector



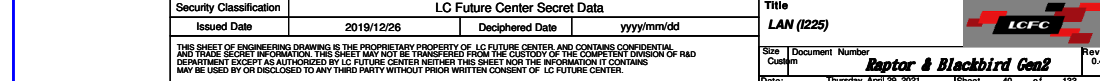
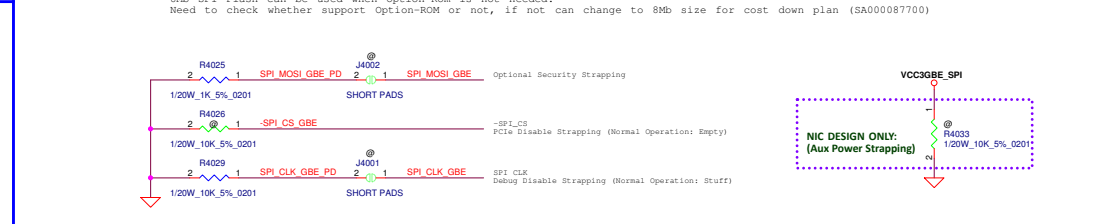
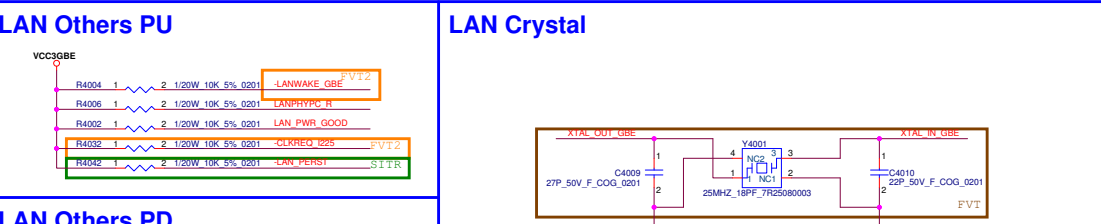
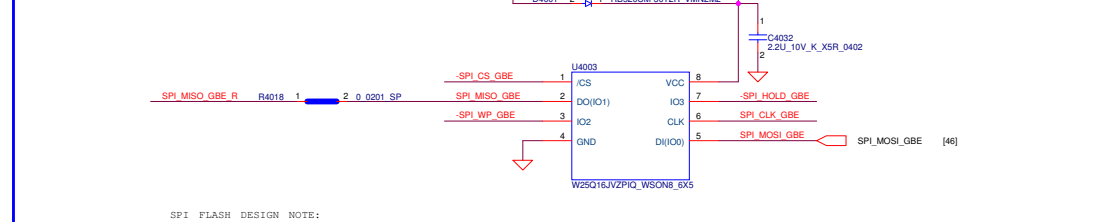
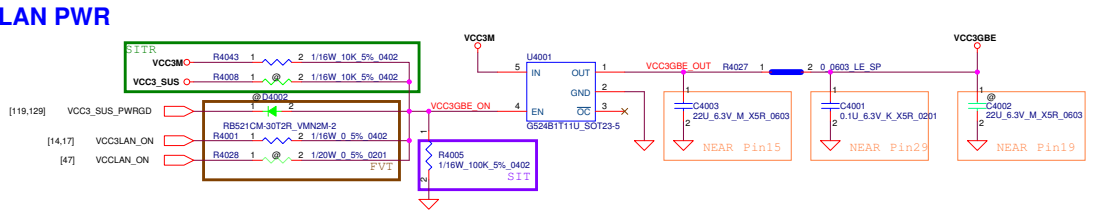
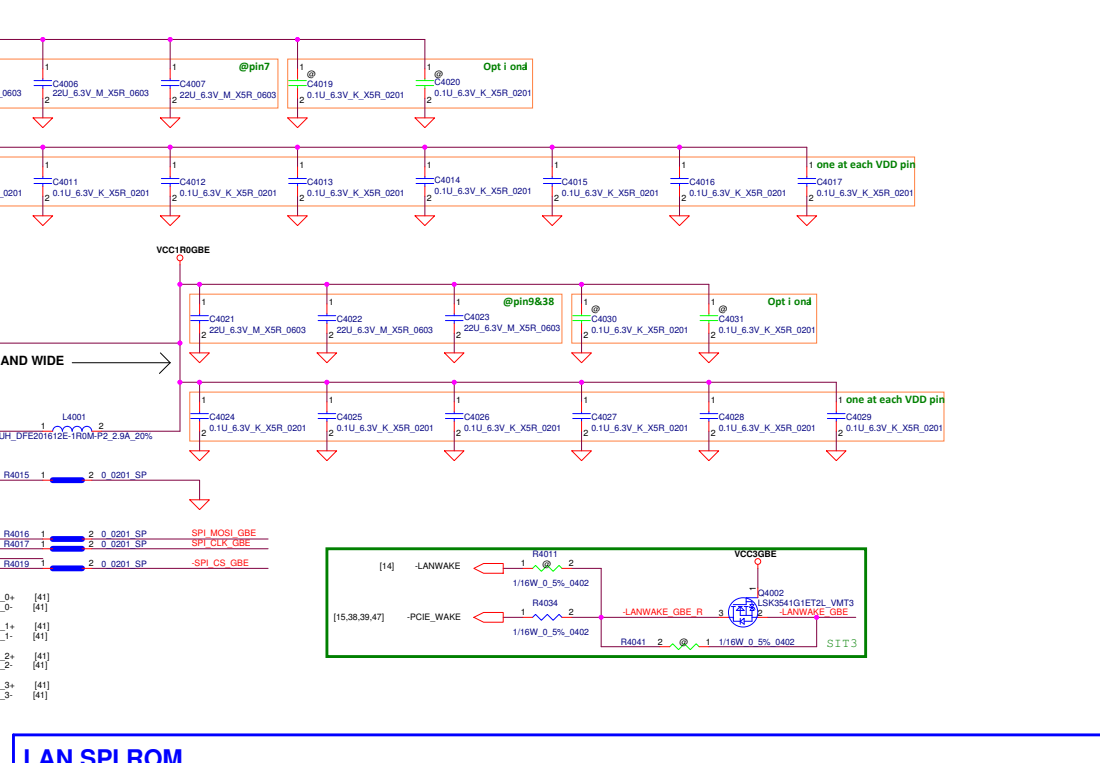
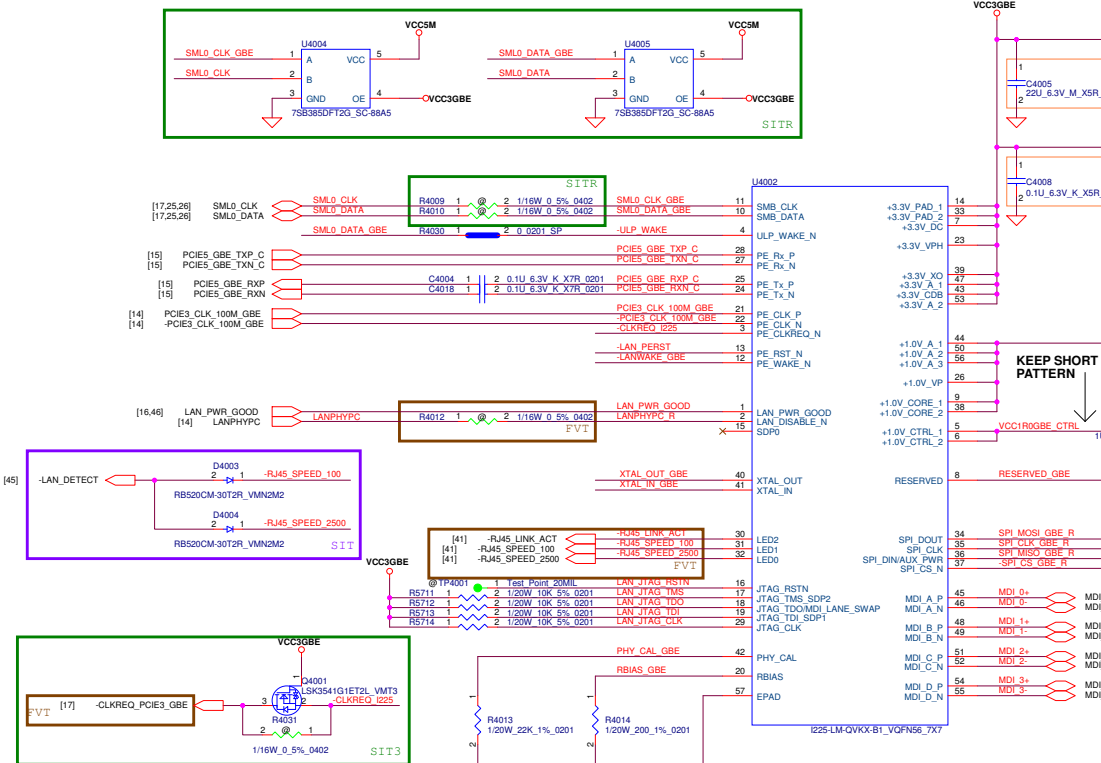
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SIM Card CONN



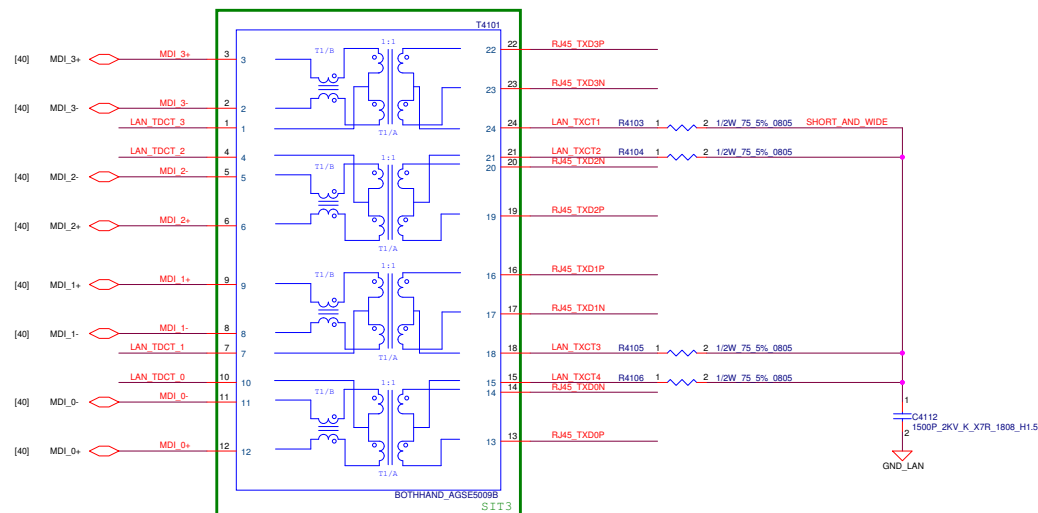
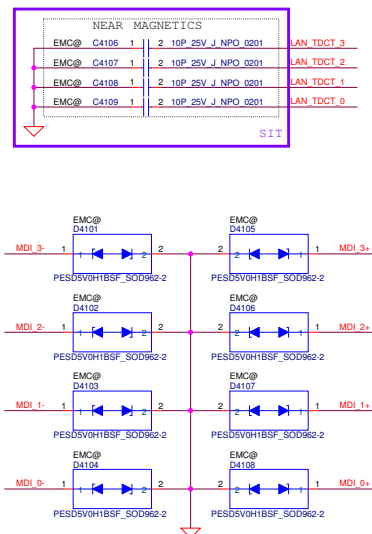
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	M2 WWAN CARD SLOT	
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Date:	Thursday, April 28, 2021	Version:	3	of	133

Intel LAN I225

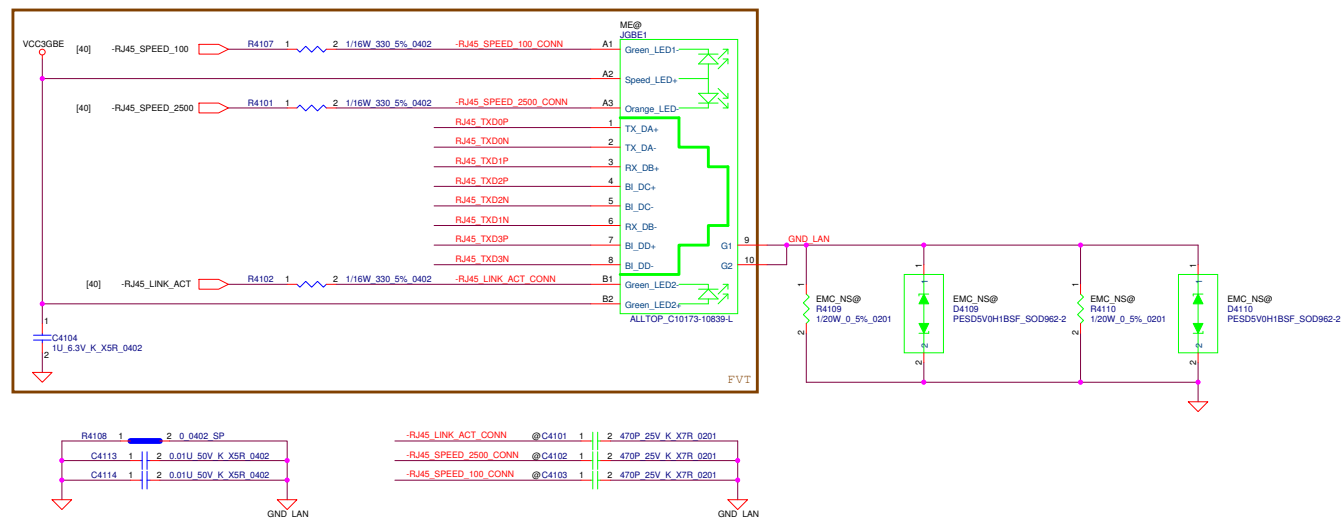



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Issued Date		2019/12/26	Deciphered Date	LAN (I225)	
			yyyy/mm/dd		
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				Raptor & Blackbird Gen2	
				Rev	0.4

2.5G Transformer

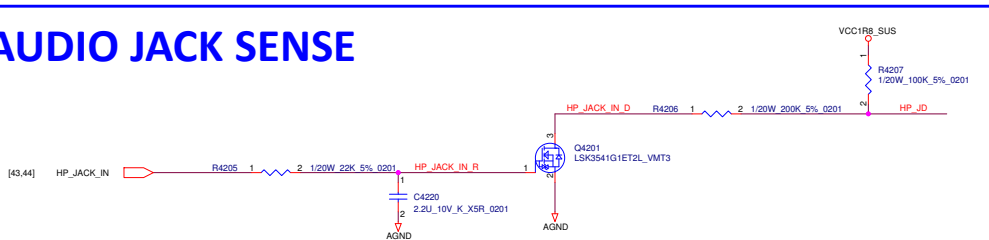
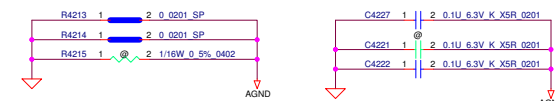
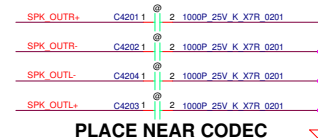



RJ45 CONN



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Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	R#45 CONNECTOR		
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AUDIO JACK SENSE



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Date:					Thursday, April 28, 2021	13:33	

NPCX997 (1/3)

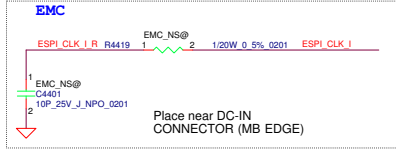
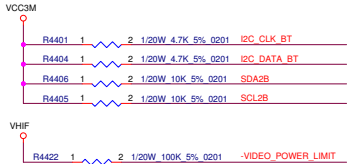
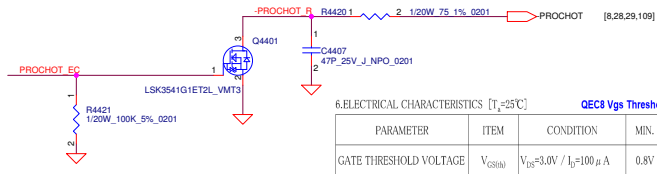
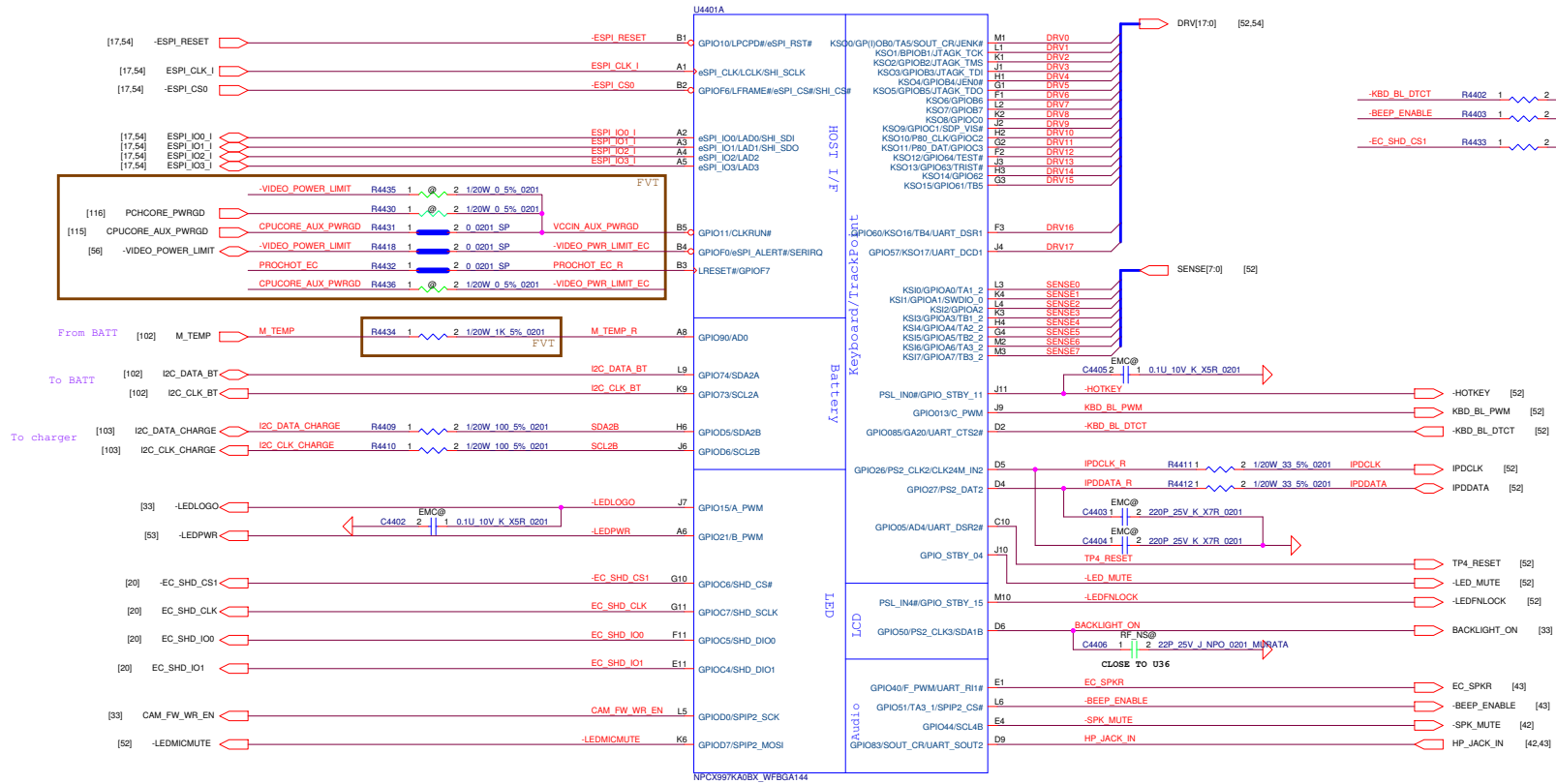
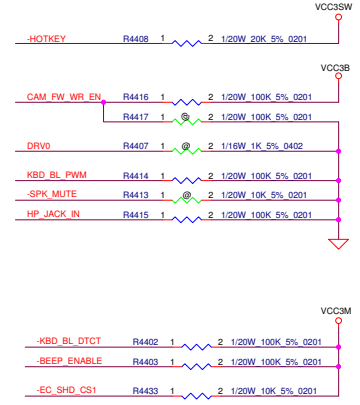


TABLE : Functional Strap

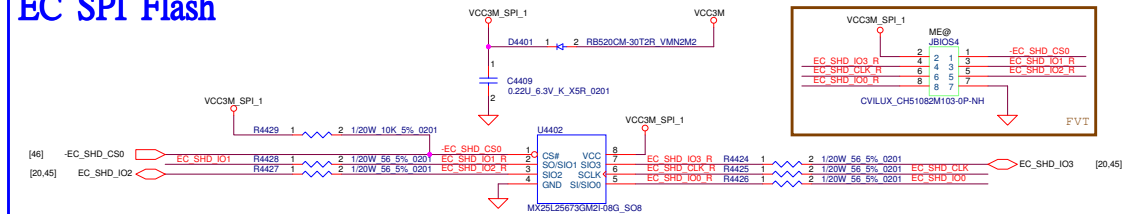
JEN1#/KSO0 (JTAG 1 Select)	
OPEN	JTAG K is disabled
LOW	JTAG K is selected



← LOGIC



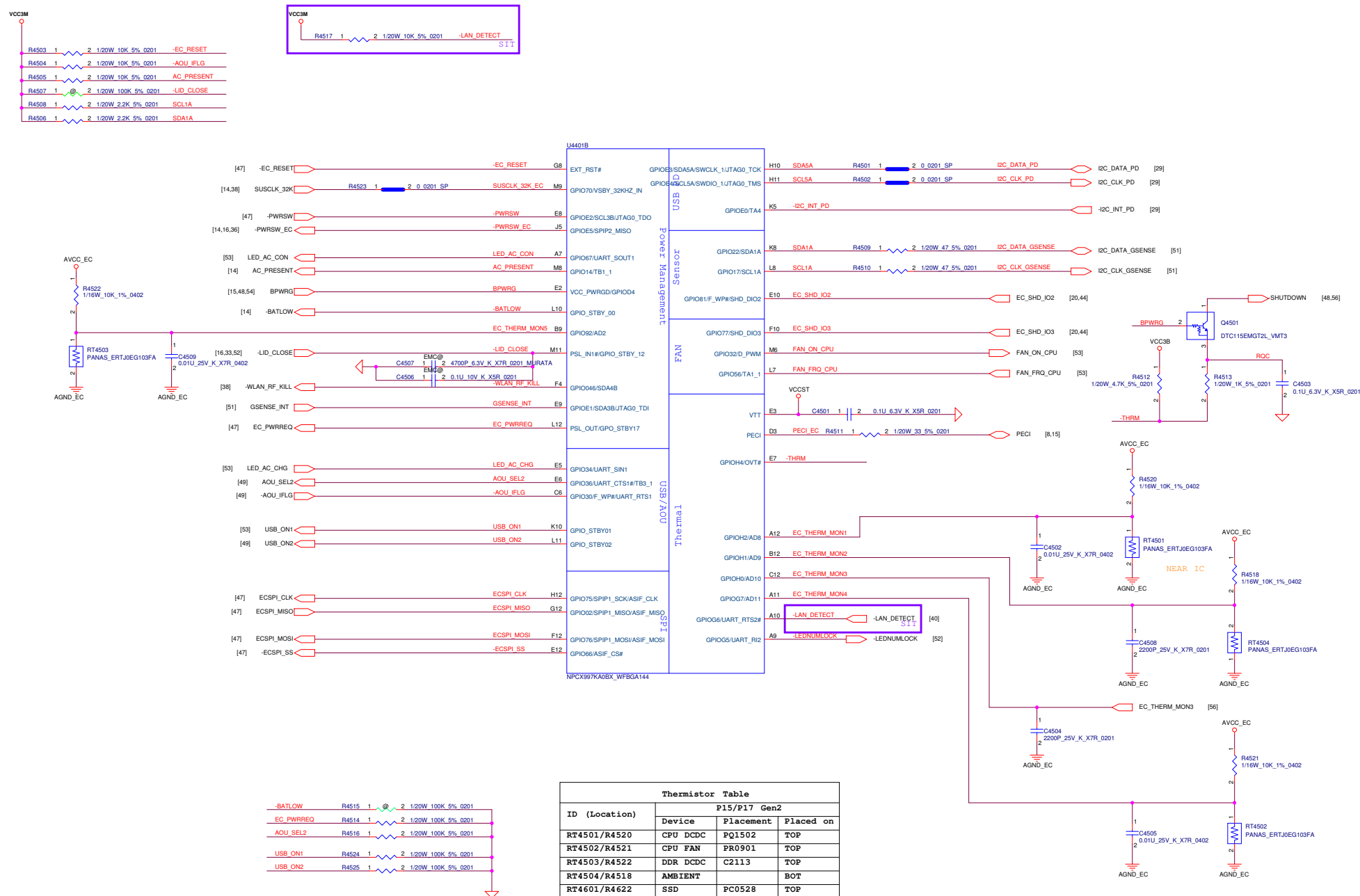
6.ELECTRICAL CHARACTERISTICS [T _a =25°C]		QEC8 Vgs Threshold voltage			
PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
GATE THRESHOLD VOLTAGE	V _{GS(th)}	V _{DS} =3.0V / I _D =100 μA	0.8V	-	1.5V

EC SPI Flash




Security Classification		LC Future Center Secret Data		Title			
Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	NPCX997KA0BX(1/3)			
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				Date: Thursday, April 26, 2021		Sheet 44 of 153	
				Raptor & Blackbird Gen 2			

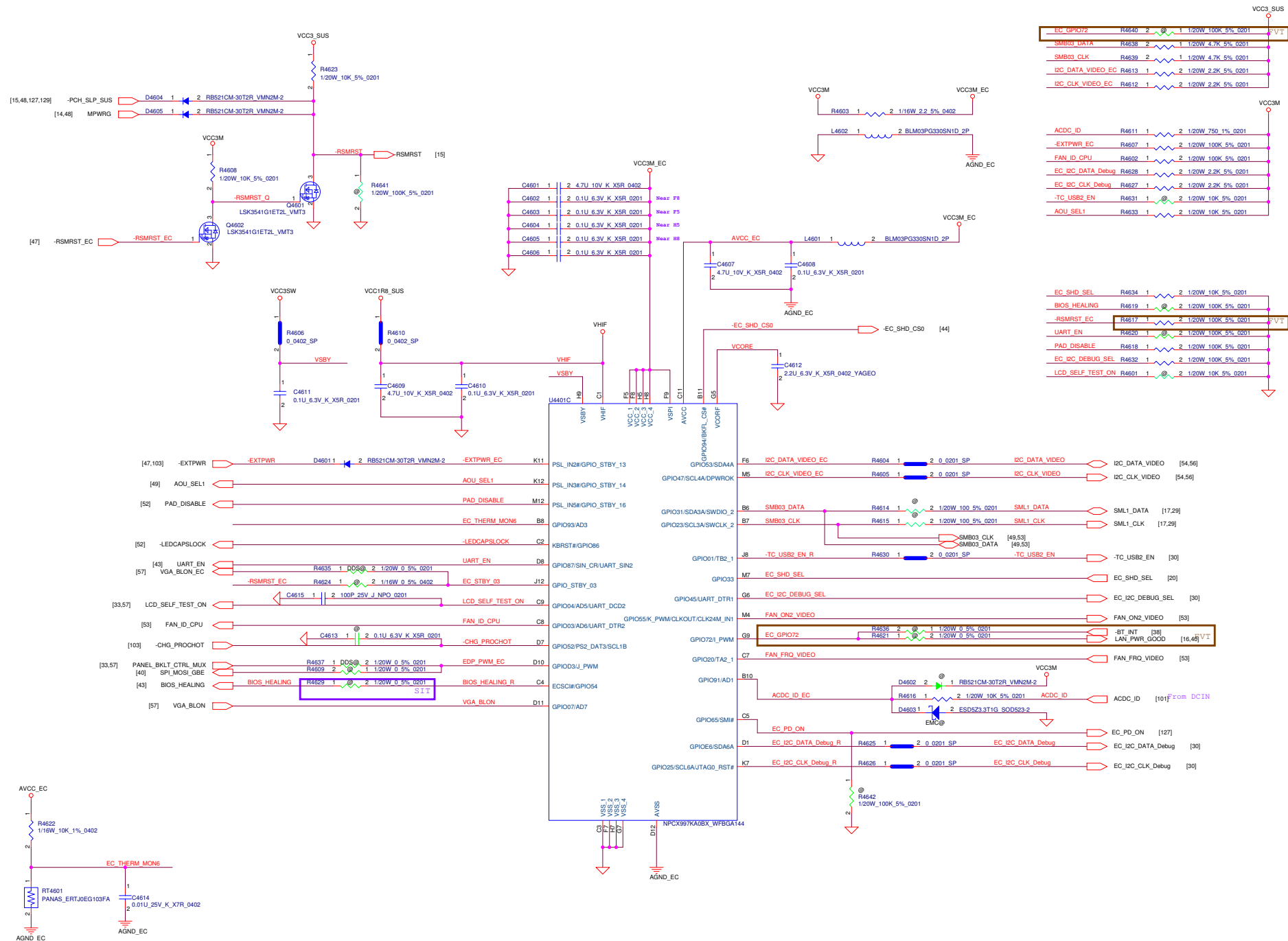
NPCX997 (2/3)




Thermistor Table			
ID (Location)	P15/P17 Gen2		
	Device	Placement	Placed on
RT4501/R4520	CPU DCDC	PQ1502	TOP
RT4502/R4521	CPU FAN	PR0901	TOP
RT4503/R4522	DDR DCDC	C2113	TOP
RT4504/R4518	AMBIENT		BOT
RT4601/R4622	SSD	PC0528	TOP

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Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	NPCC997KA0BX(2/3)		
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				Size	Document Number	Rev
				Date	Daptor & Blackbox	0.4
				Thursday, April 26, 2024	133	

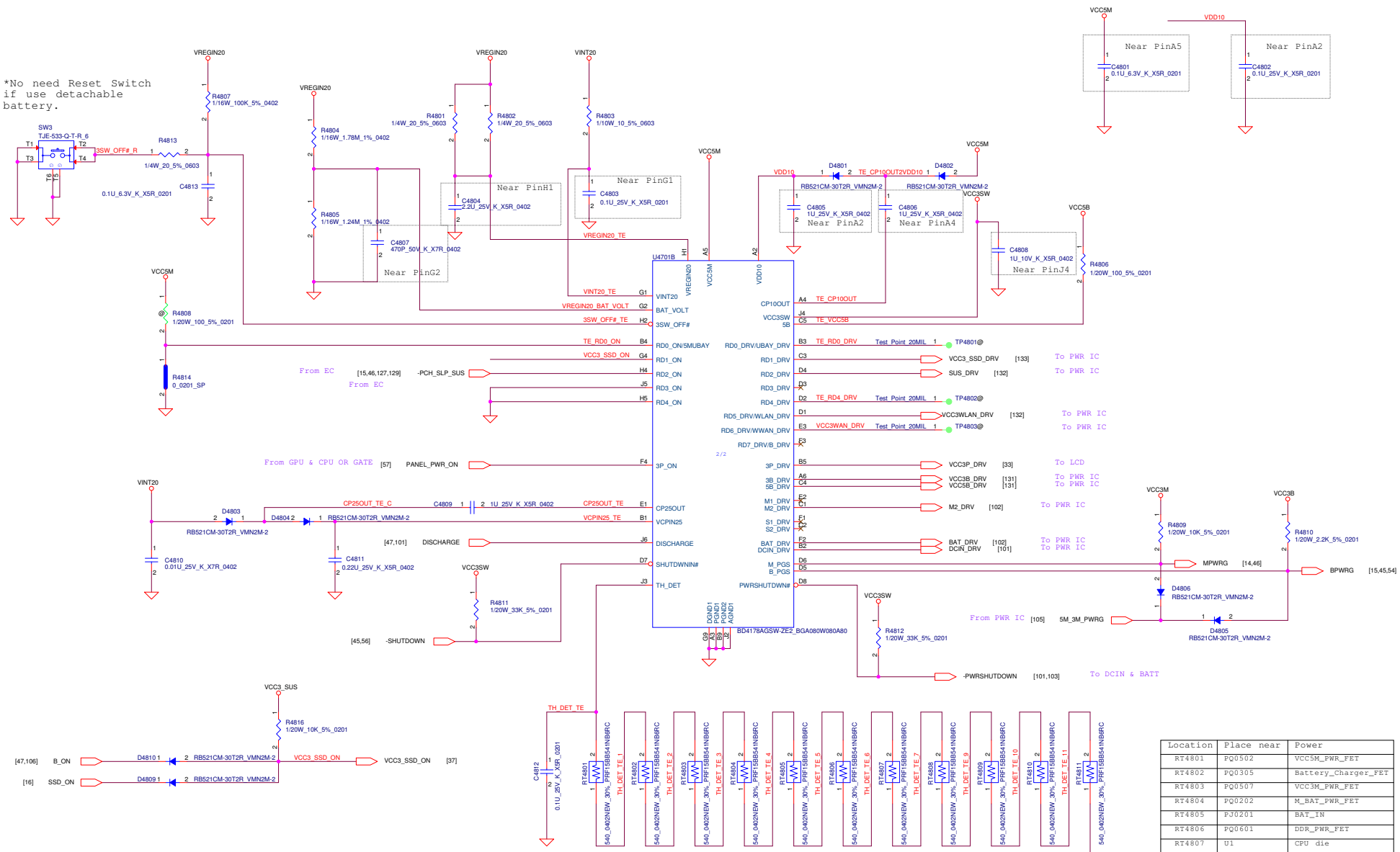
NPCX997 (3/3)



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Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	NPCC997KA0BX(3/3)	
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THINK ENGINE

*No need Reset Switch
if use detachable
battery.



Location	Place near	Power
RT4801	PQ0502	VCC5M_PWR_FET
RT4802	PQ0305	Battery_Charger_FET
RT4803	PQ0507	VCC3M_PWR_FET
RT4804	PQ0202	M_BAT_PWR_FET
RT4805	PJ0201	BAT_IN
RT4806	PQ0601	DDR_PWR_FET
RT4807	U1	CPU die
RT4808	PJ1003	VCCCPUCORE_DR.MOS_2
RT4809	PQ1501	VCCCPUCORE_AUX_FET
RT4810	PQ0102	DCIN_PWR_FET
RT4811	PQ1601	VCCPCRCORE_FET

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2019/12/26		yyyy/mm/dd									
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						<small>Custom</small>					
<small>Date:</small>						<small>Thursday, April 25, 2021</small>		<small>Sheet</small>	<small>50</small>	<small>of</small>	<small>153</small>

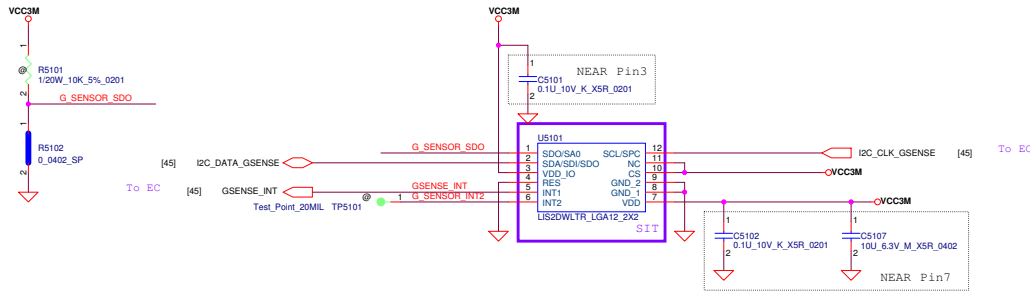
G-SENSOR

TABLE

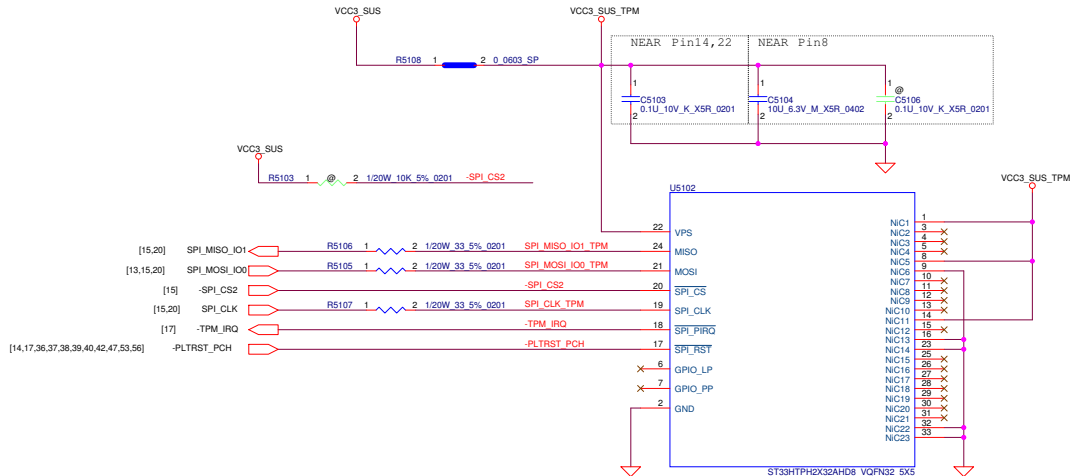
Vendor	ADDR_SEL	Address
ST	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
BOSCH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

TABLE of G-Sensor

Vendor	Mfr. P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA280	SA0000A1600



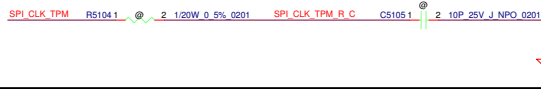
DISCRETE TPM 2.0



TABLE

Pin No	NUVOTON NPCT750LADYX SA00008KS30	ST Micro ST33HTPH2X32AHD8 SA0000AB720
1	VDD	NC
2	NC	NC
3	NC	NC
4	PP	NC
5	NC	NC
6	GPIO3	GPI
7	NC	PP
8	VDD	NIC
9	NC	NC
10	NC	NC
11	NC	NC
12	NC	NC
13	GPIO4	NC
14	NC	NC
15	NC	NC
16	GND	NC
17	RST#	SPI_RST#
18	PIRQ#	SPI_PIRQ#
19	SCLK	SPI_CLK
20	CS#	SPI_CS#
21	MOSI	MOSI
22	VDD	VPS
23	GND	NC
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	SDA/GPIO0	NC
30	SCL/GPIO1	NC
31	NC	NC
32	NC	NC

EMC



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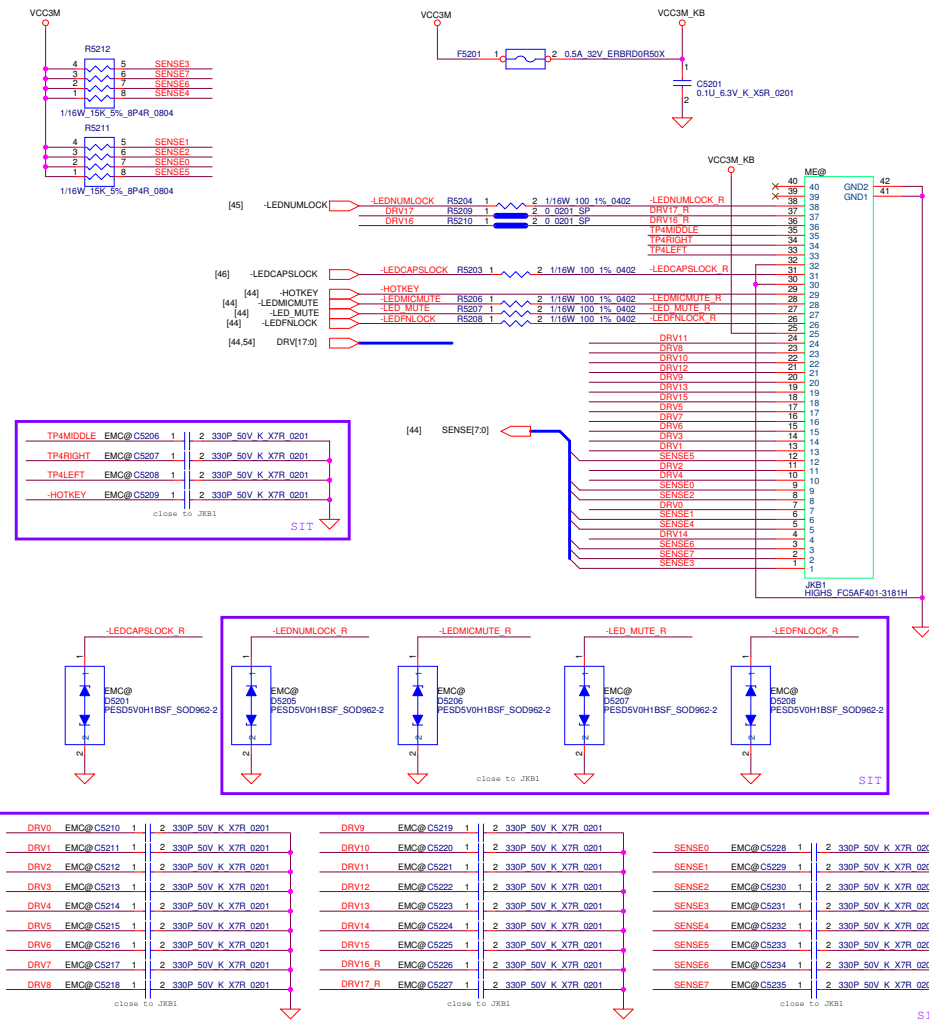
TABLE of TPM (U42)

Vendor	P/N	LCFC P/N	Valid through
NUVOTON	NPCT750LADYX	SA00008KS30	
ST	ST33HTPH2X32AHD8	SA0000AB720	

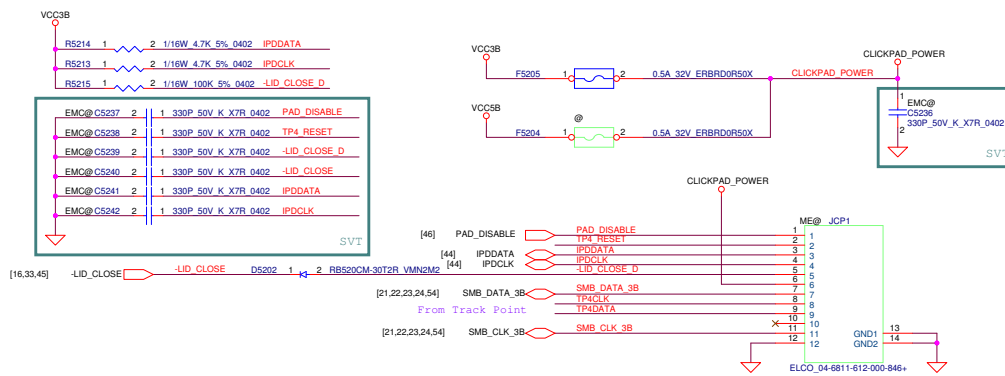
Security Classification	LC Future Center Secret Data			Title
Issued Date	2019/12/26	Deciphered Date	yyyy/mm/dd	APS G-SENSOR
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Date: Thursday, April 25, 2021				Document Number Rev 0.4

LCFC		Raptor & Blackbird Gen2	
Sheet	01	Rev	0.4

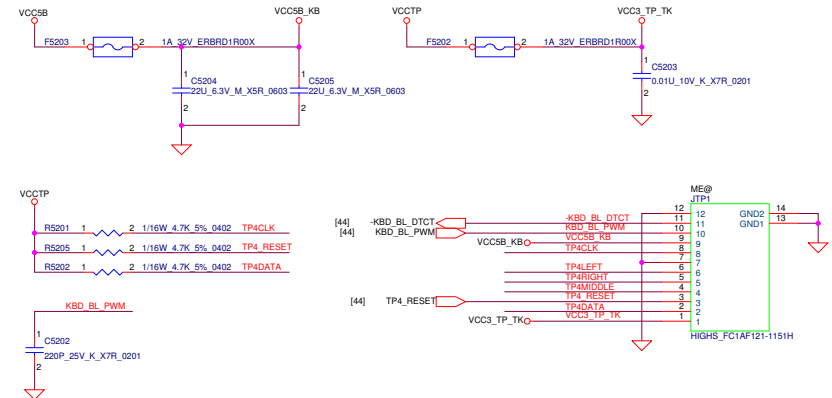
KEYBOARD



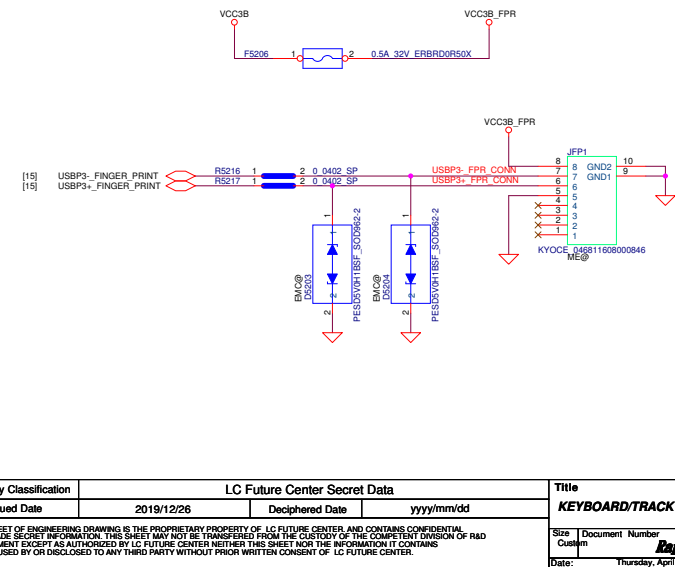
CLICK PAD




TRACK POINT

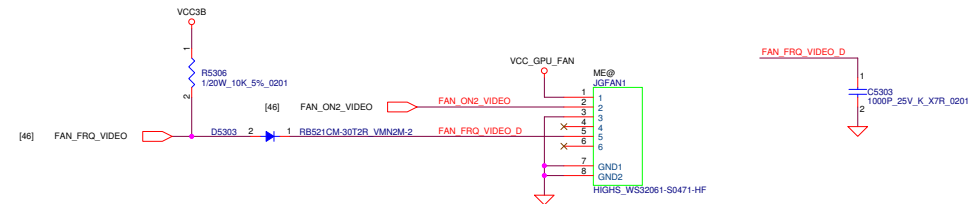


Finger Print

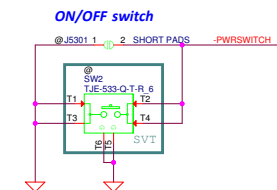


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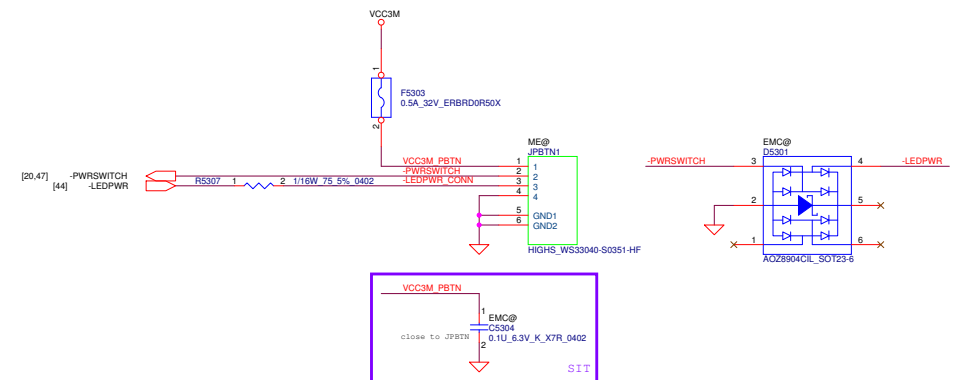
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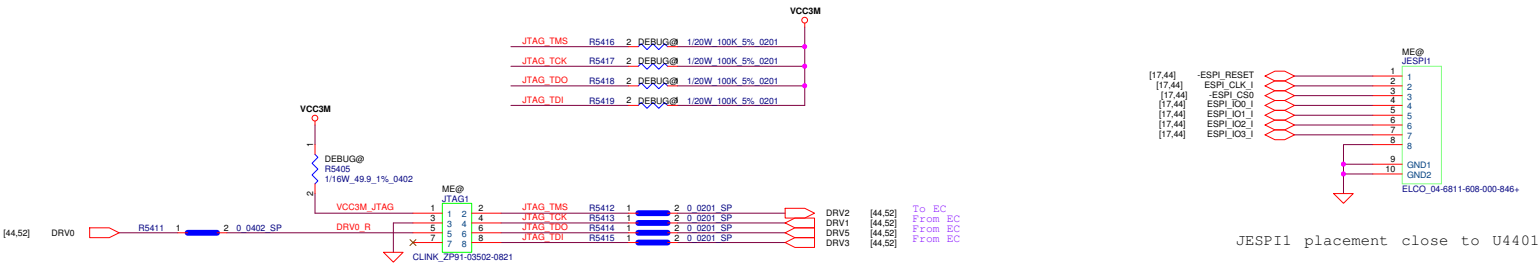
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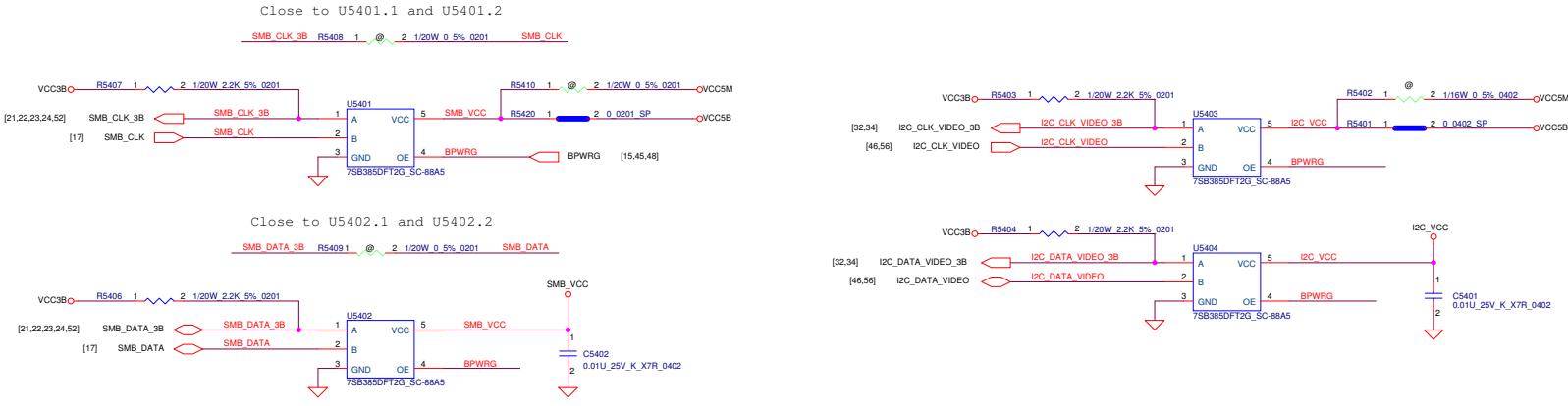
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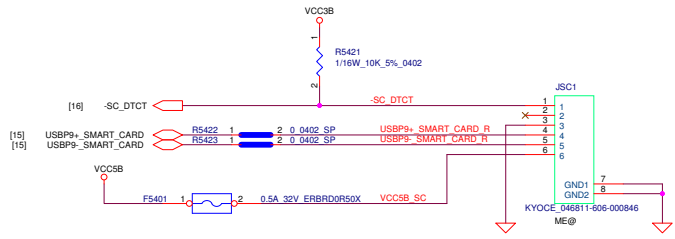
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SMBUS SWITCH



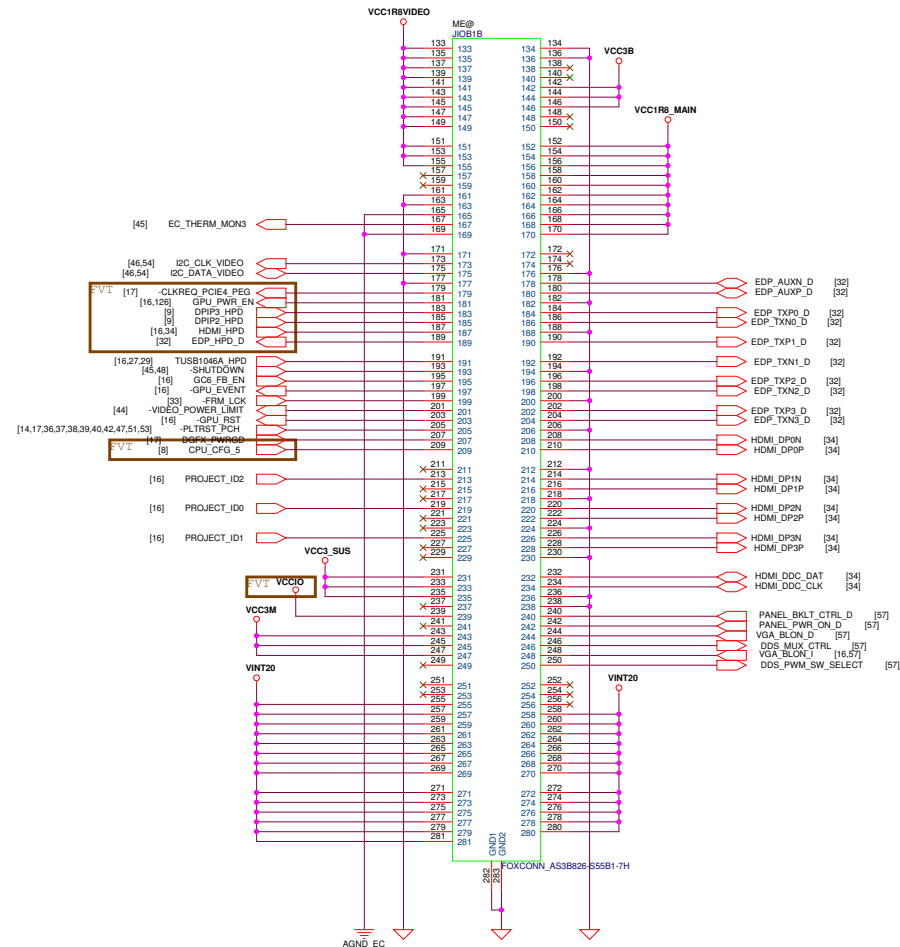
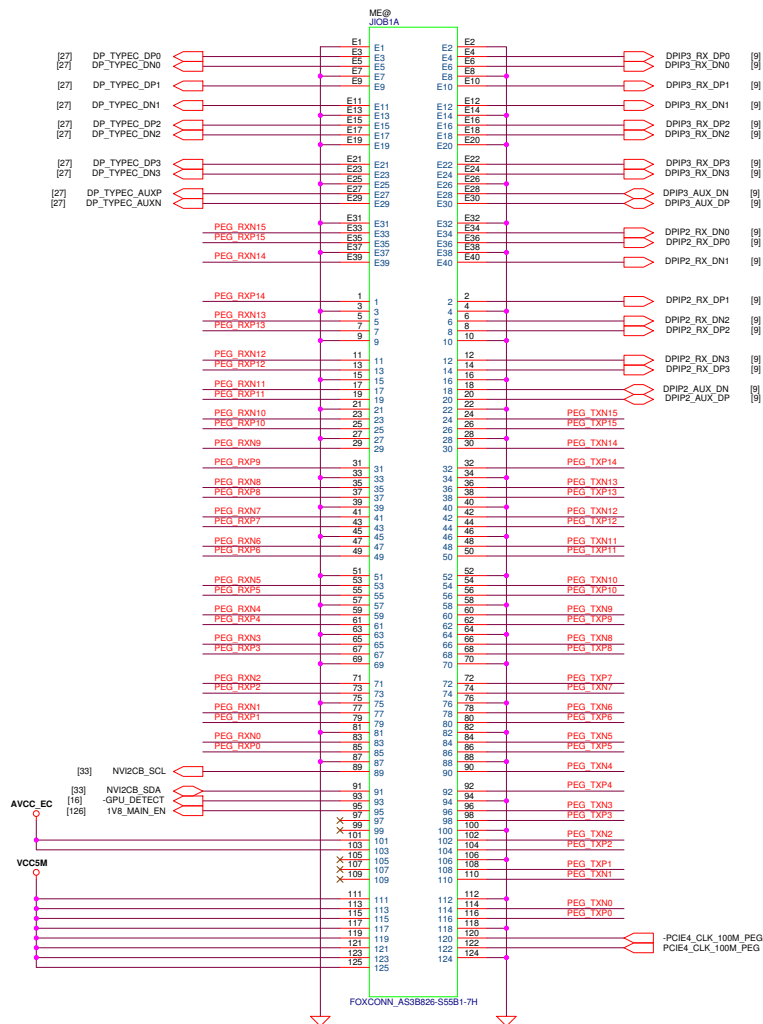
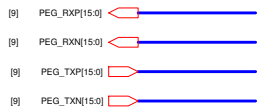
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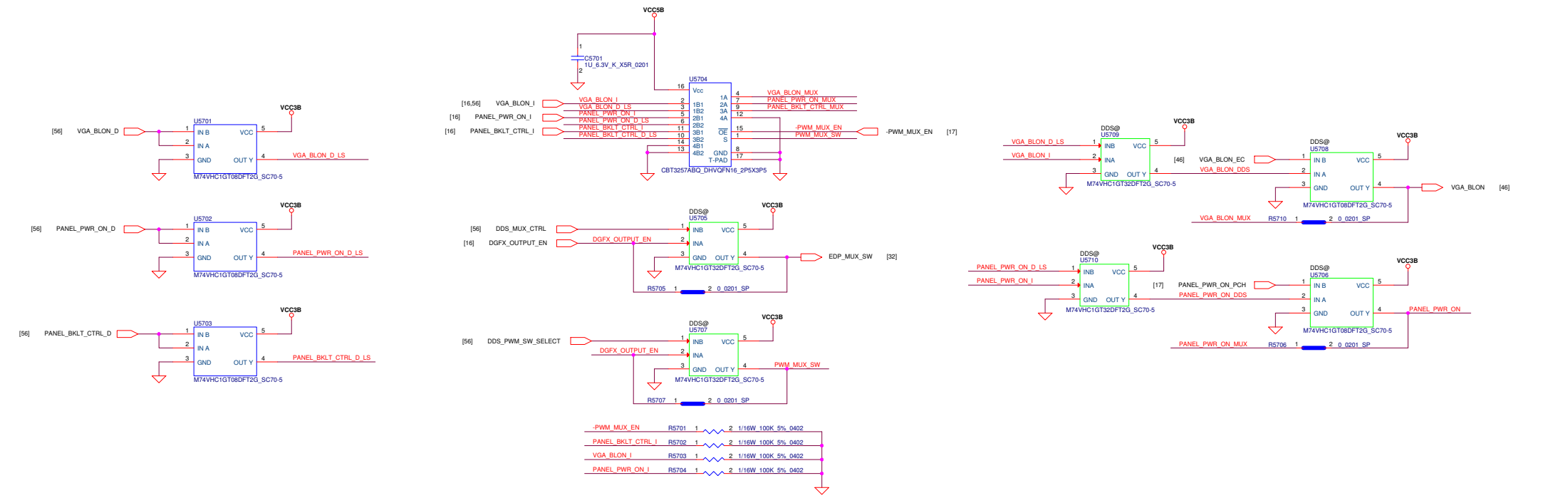
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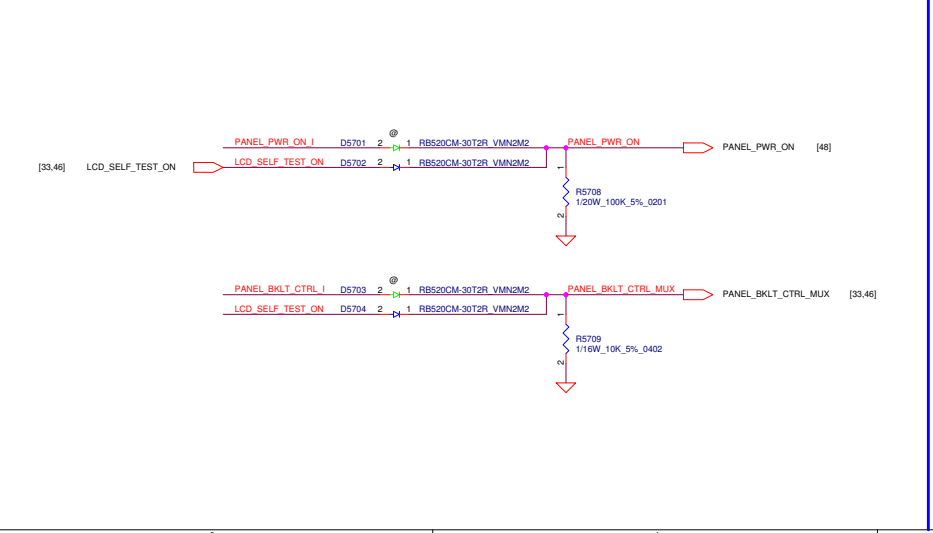


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eDP Switch




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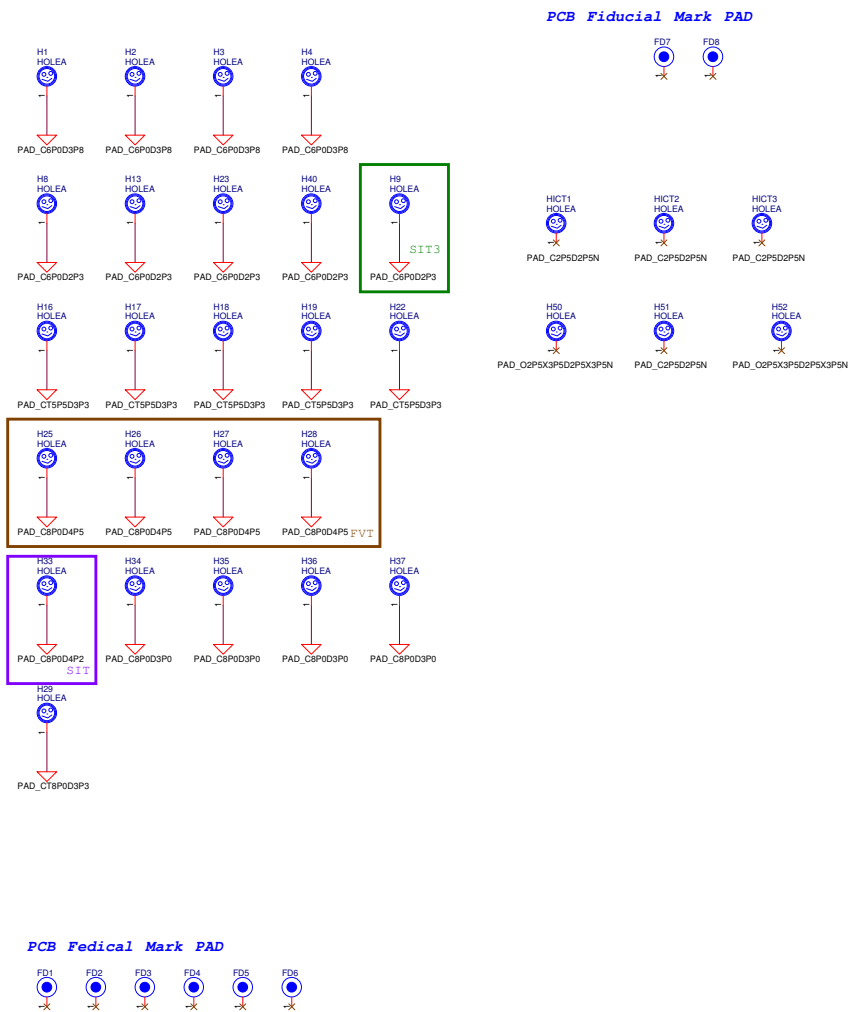
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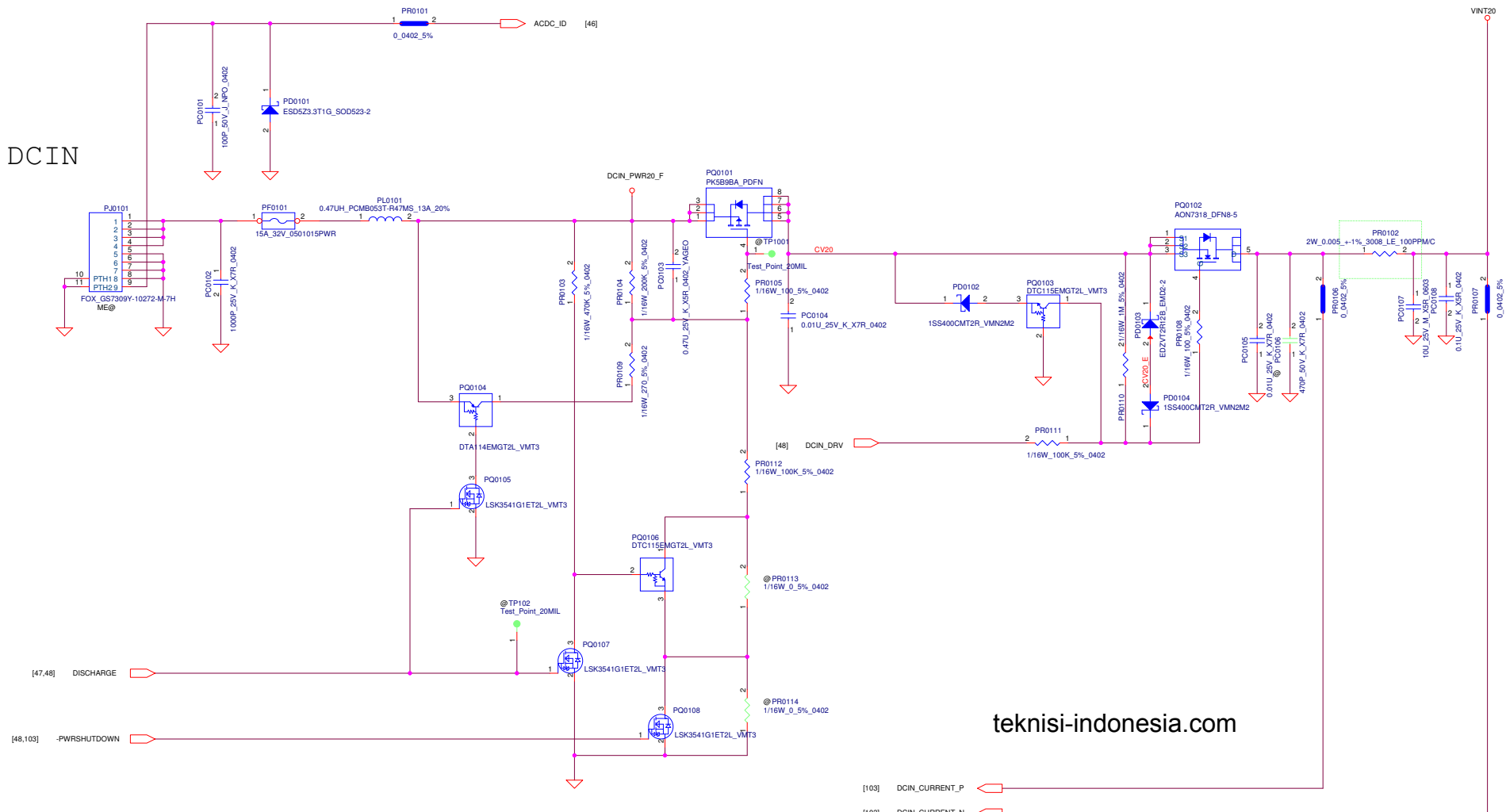
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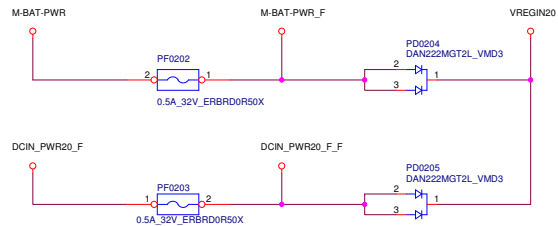
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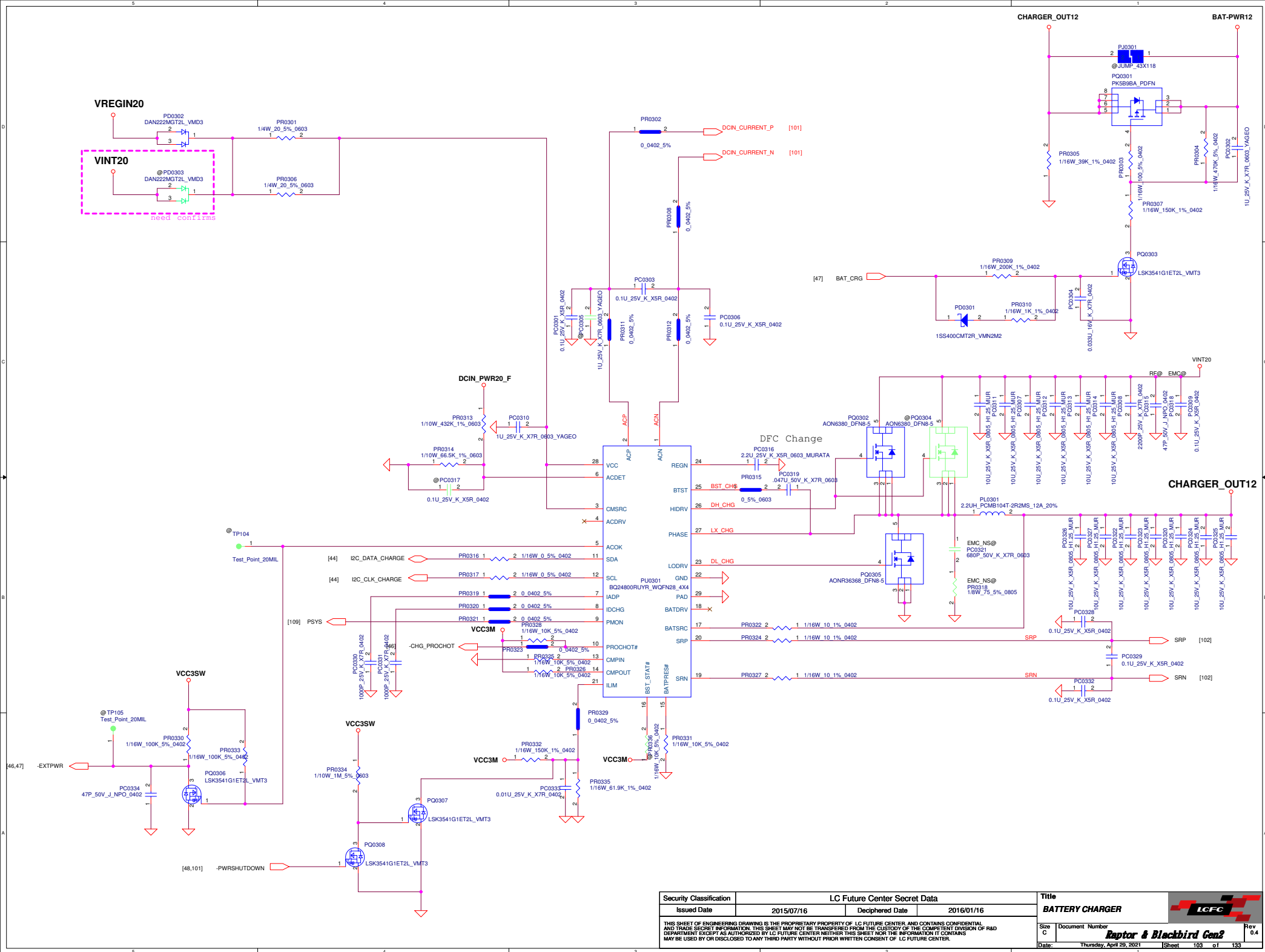
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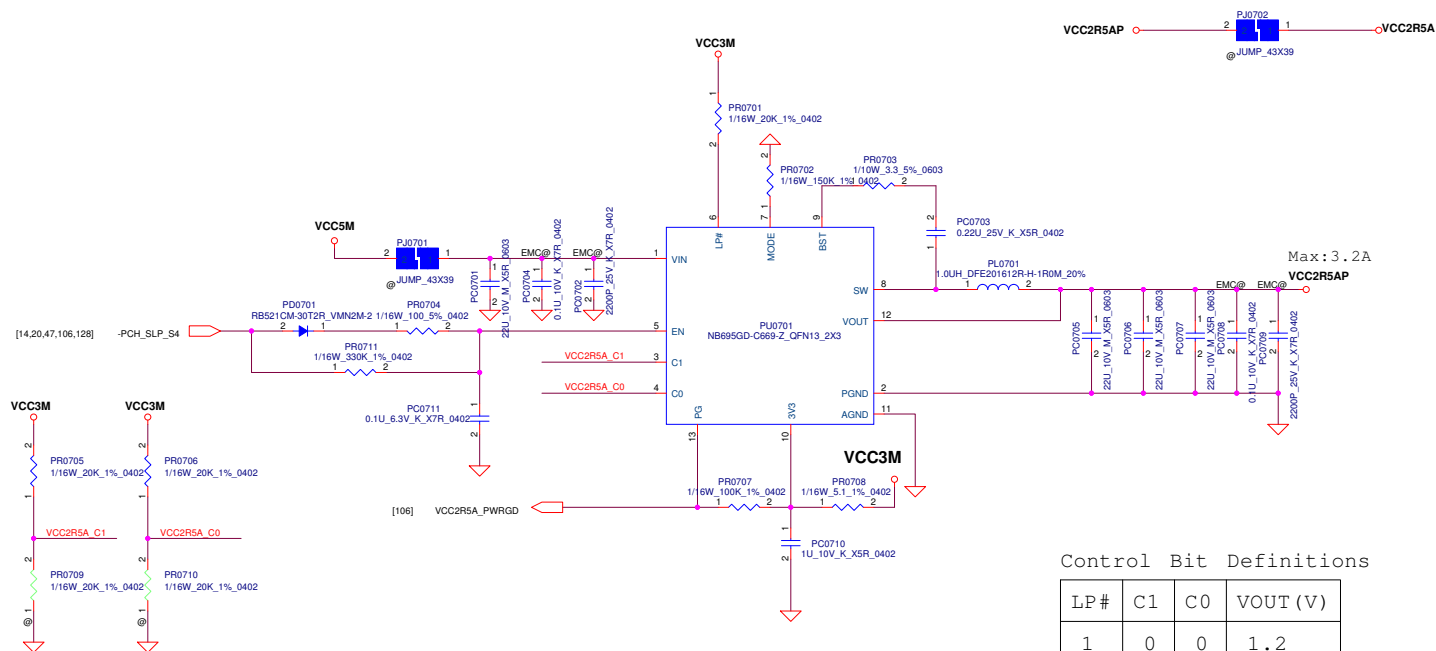
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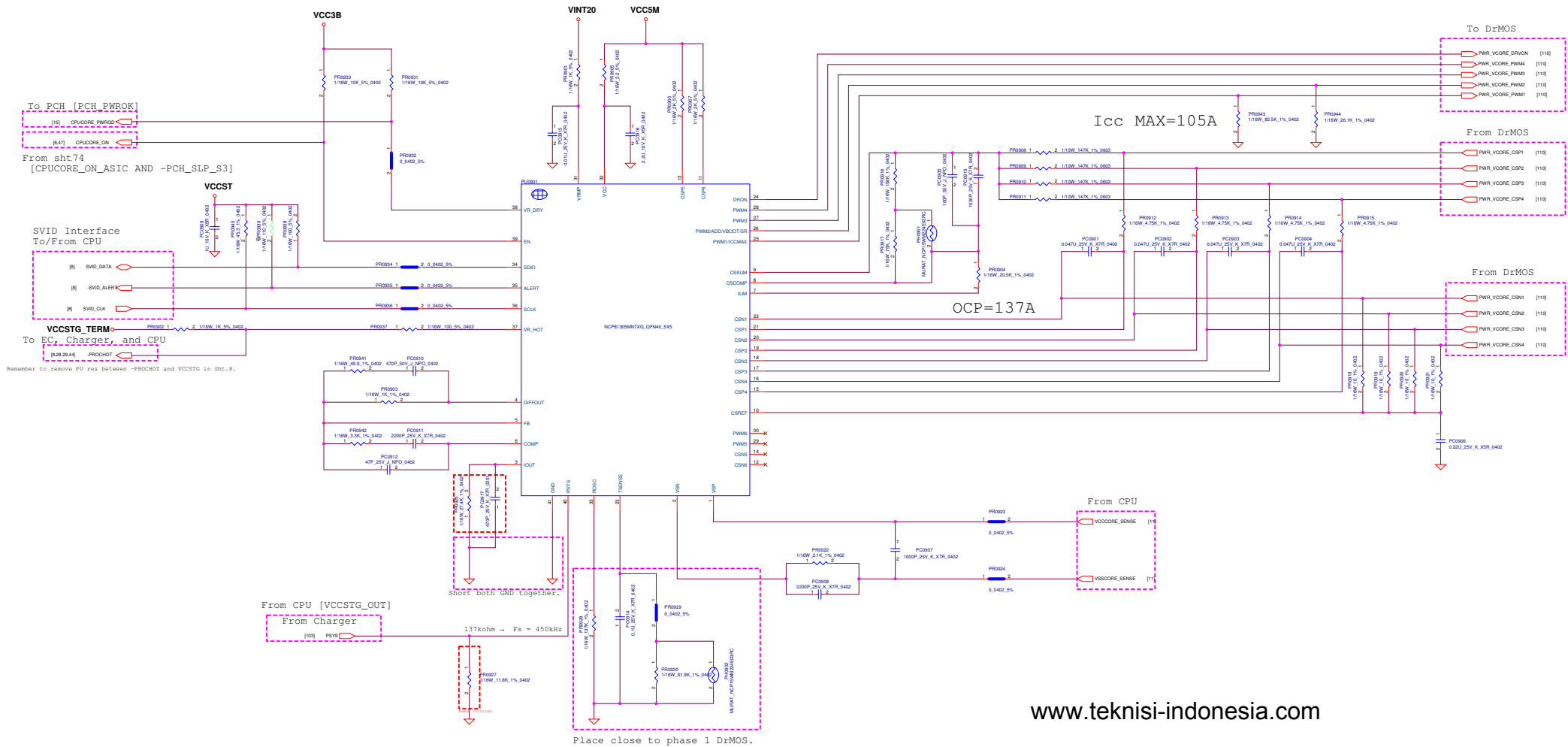
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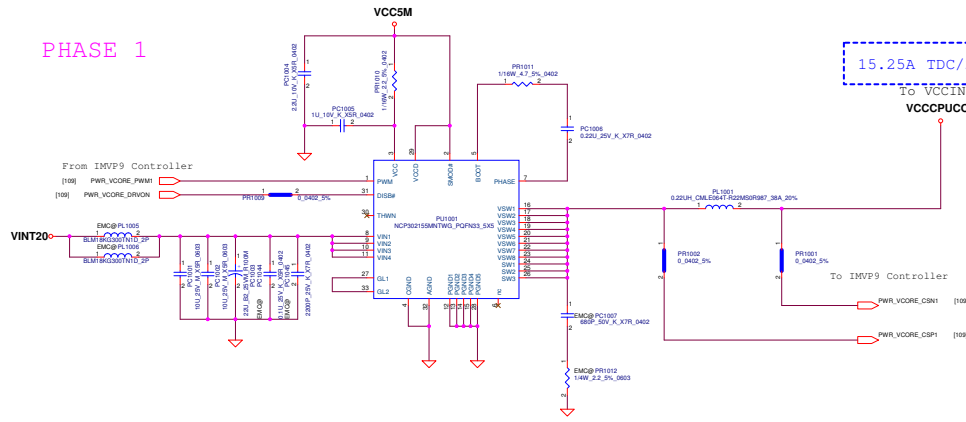


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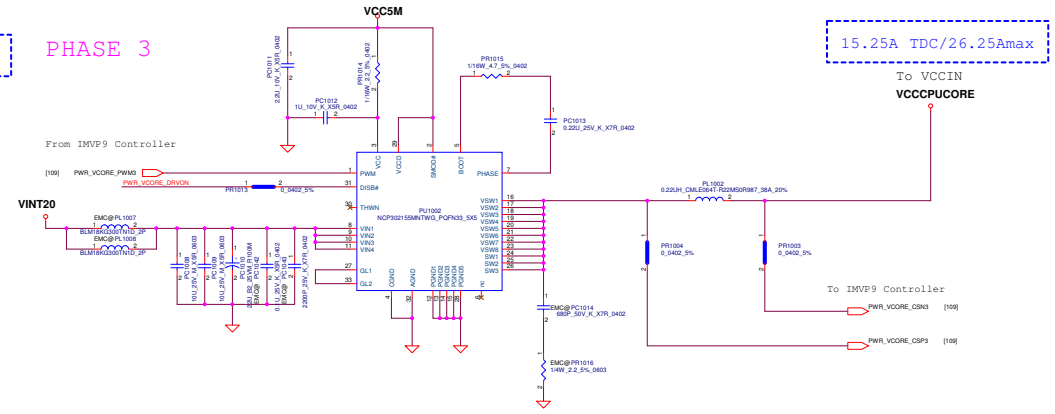


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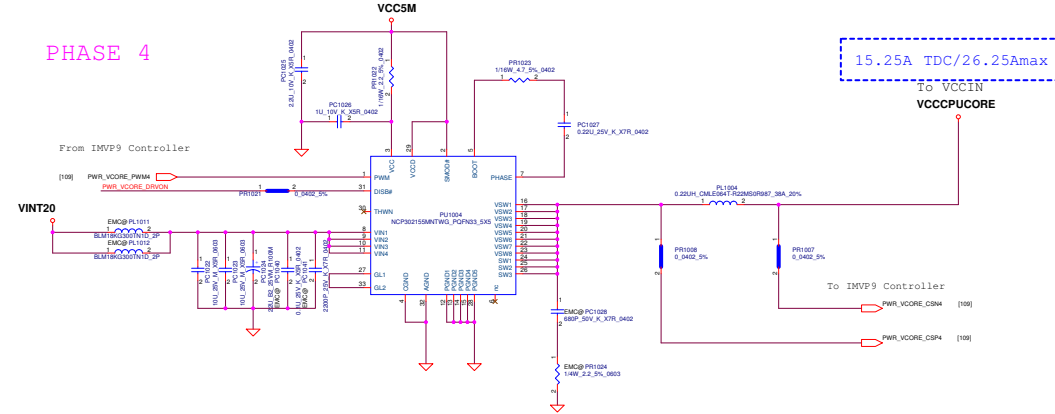


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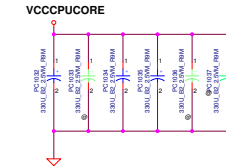
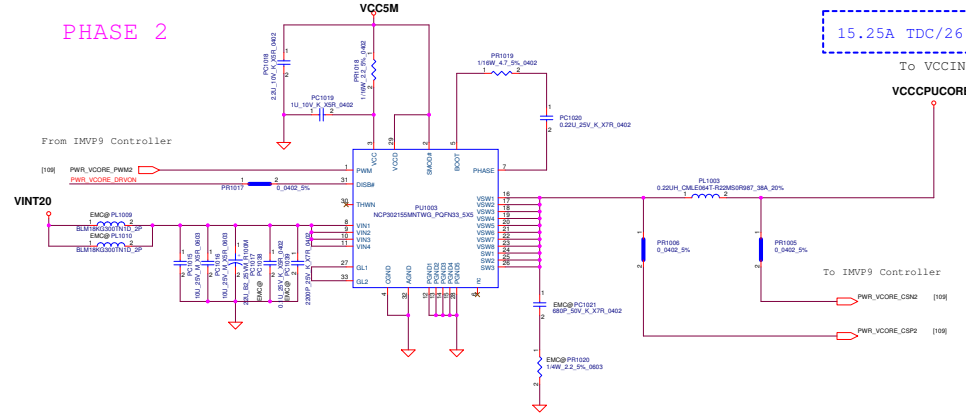
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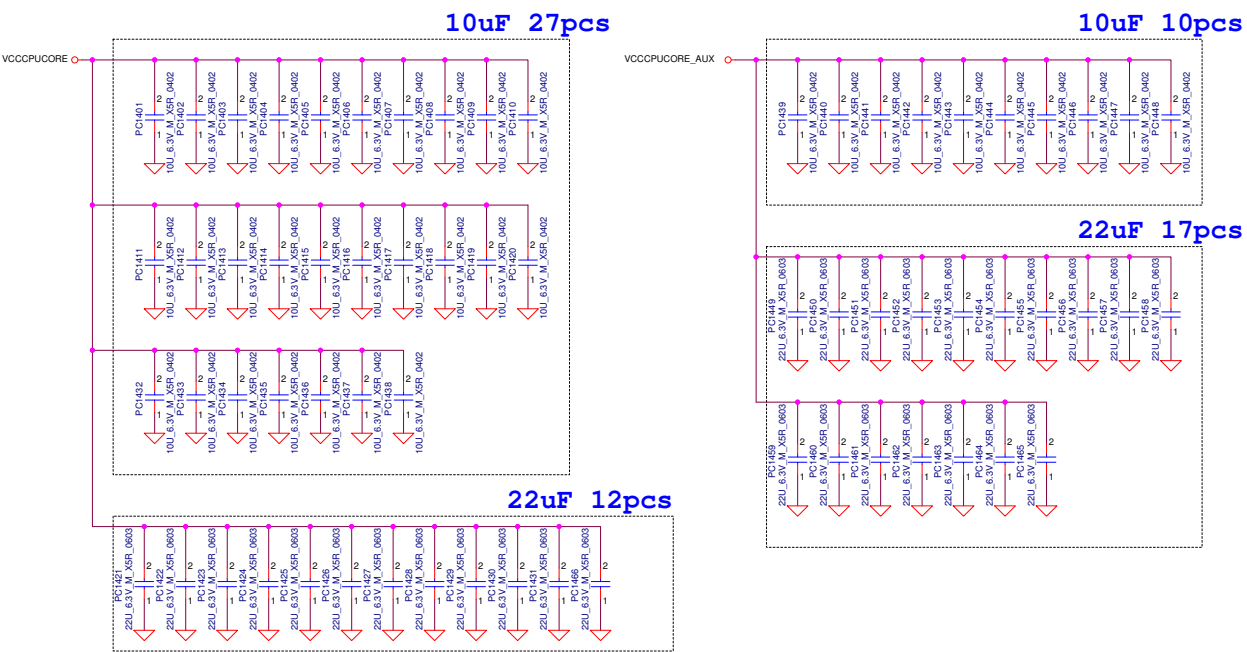
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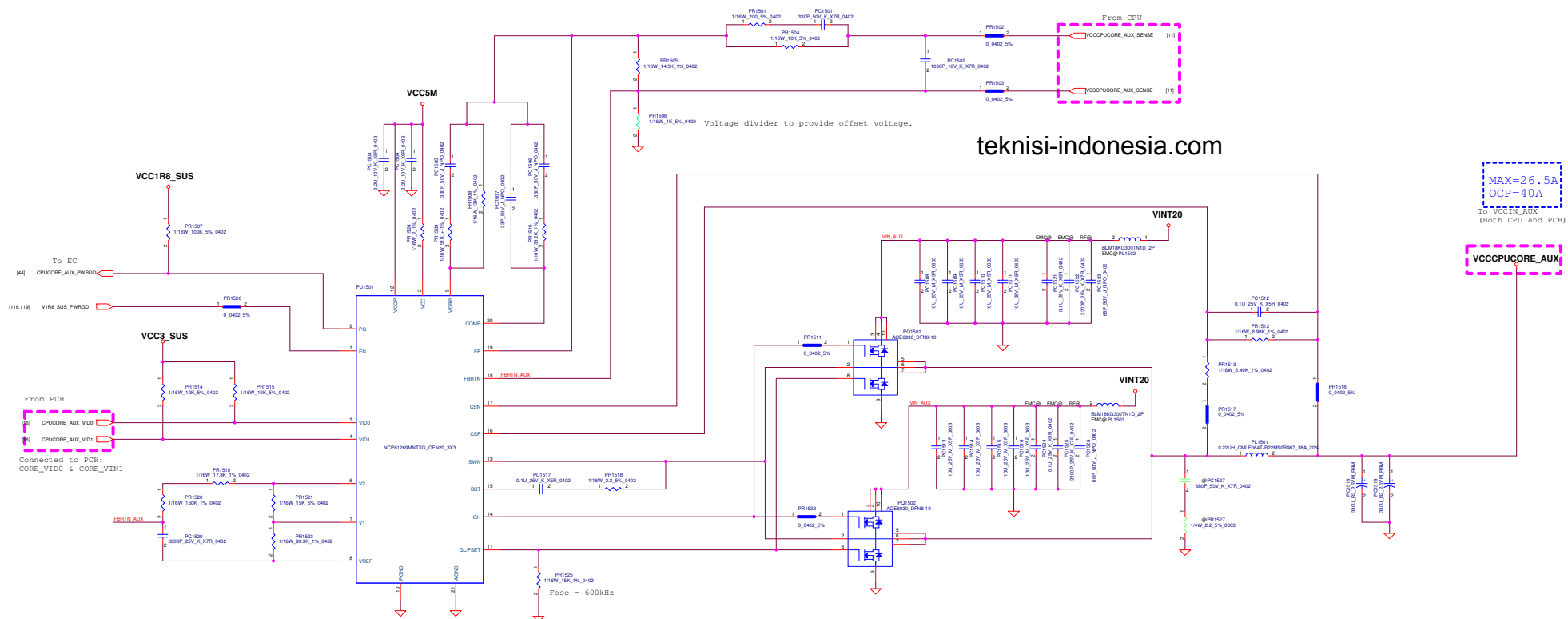
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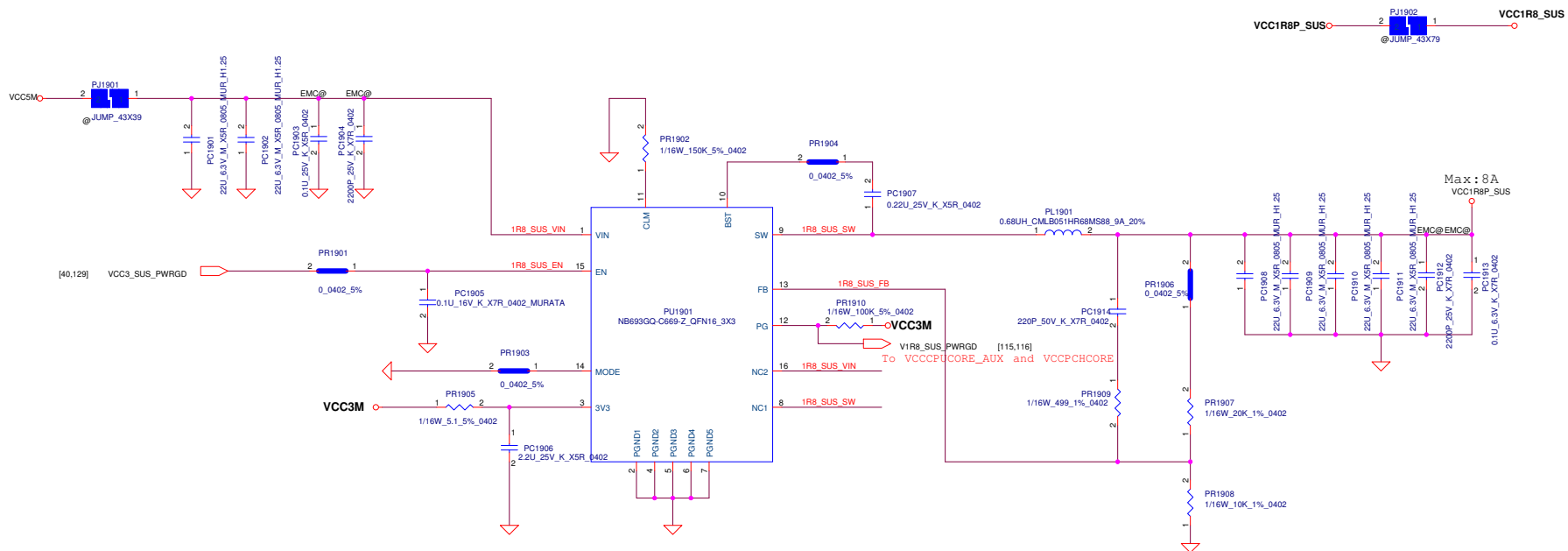
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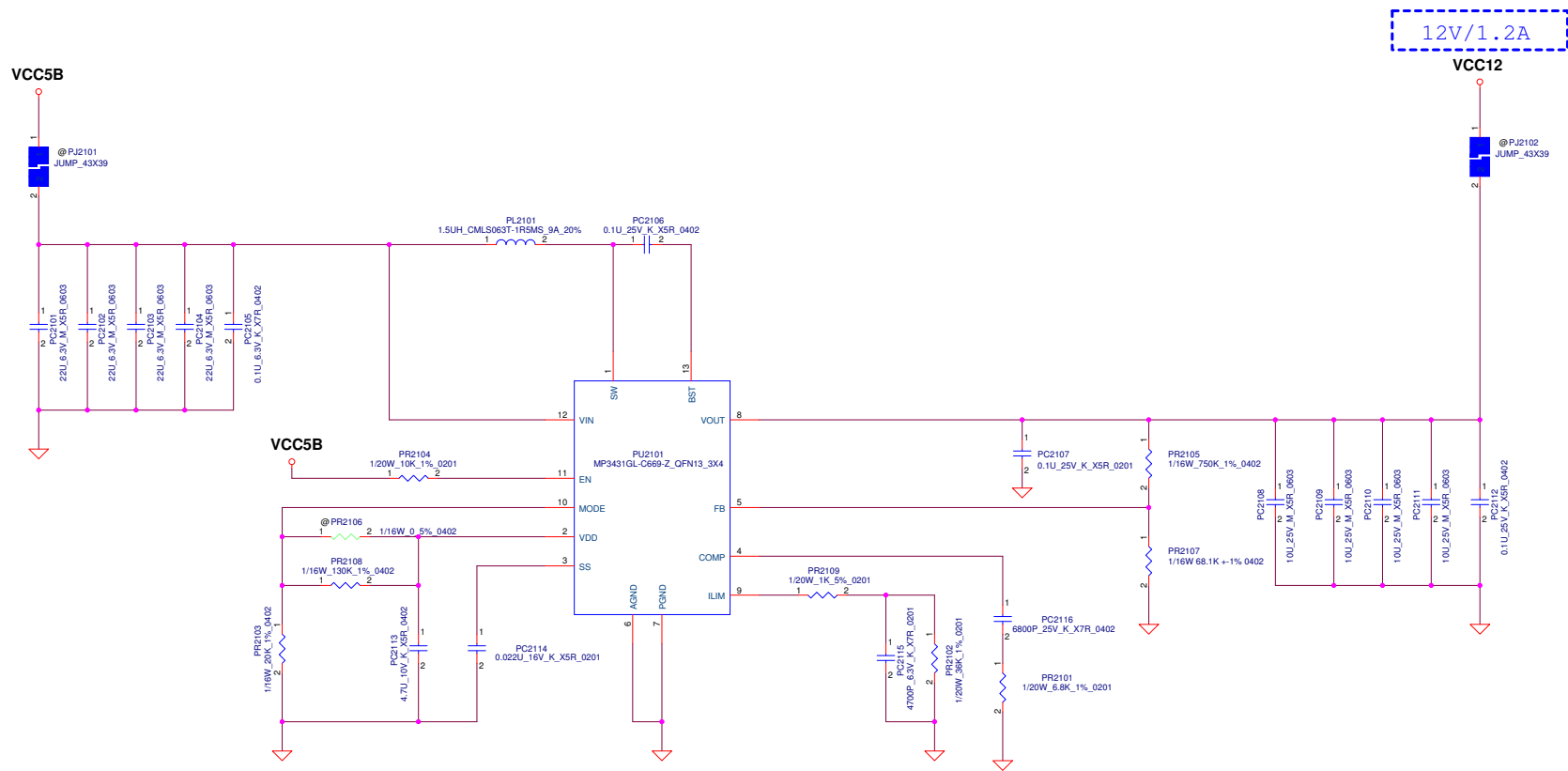


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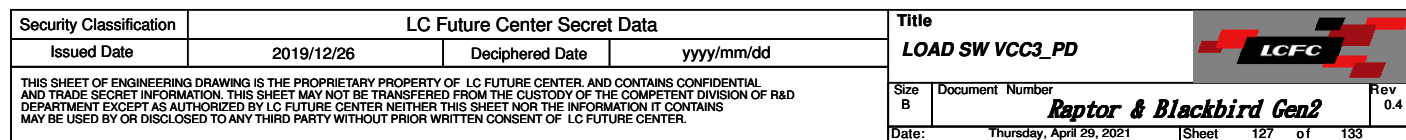
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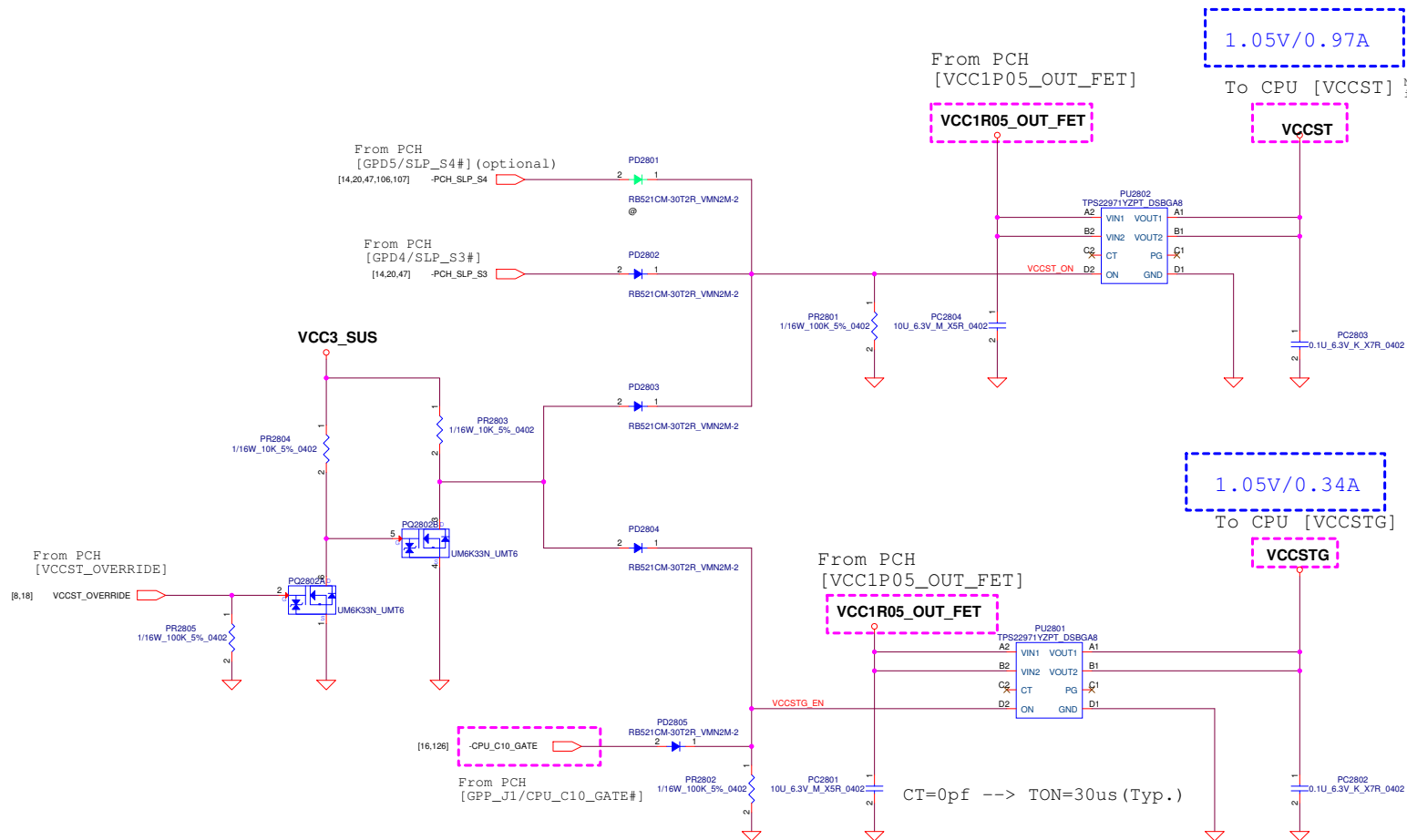
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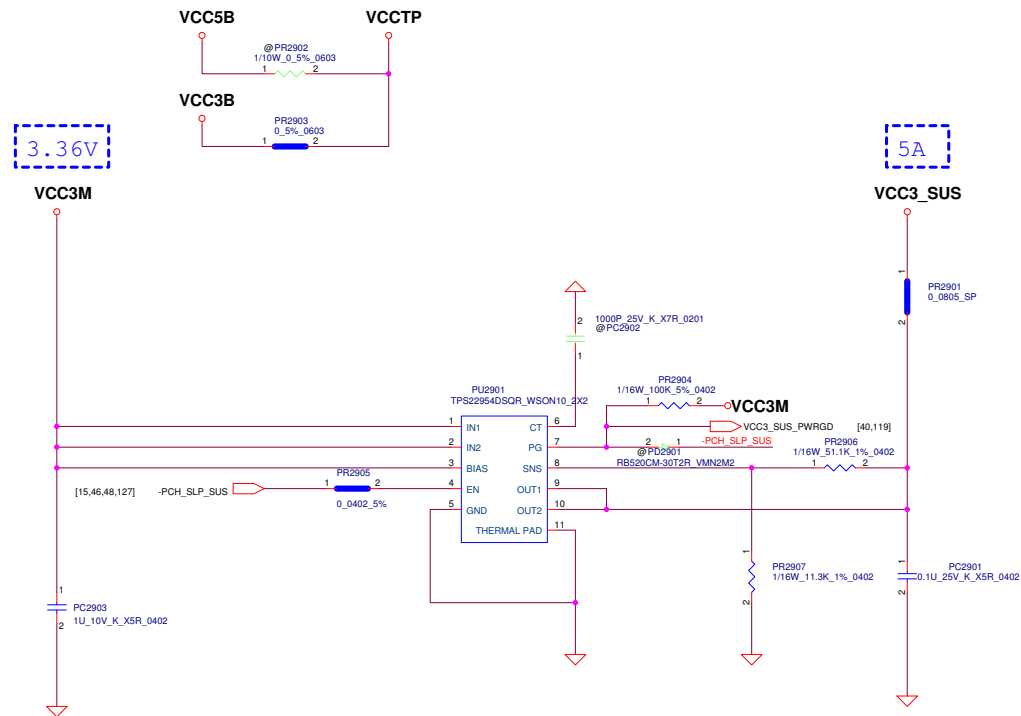
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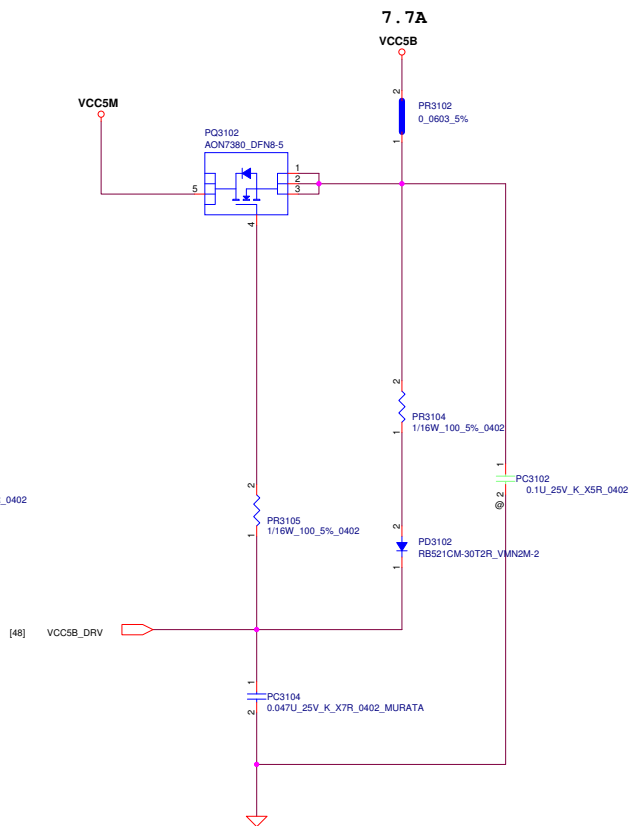
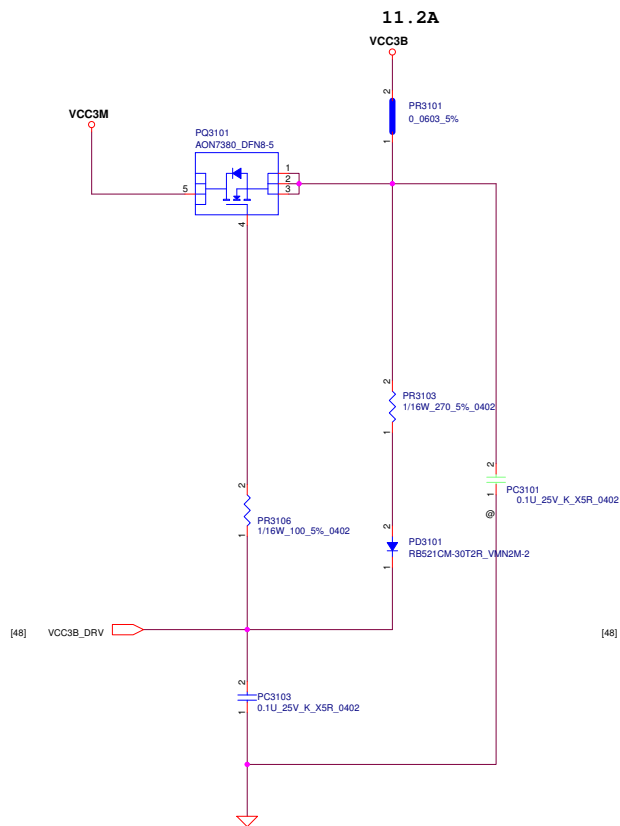
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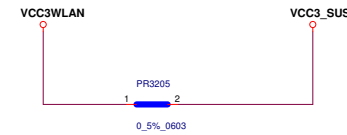
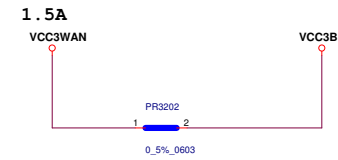
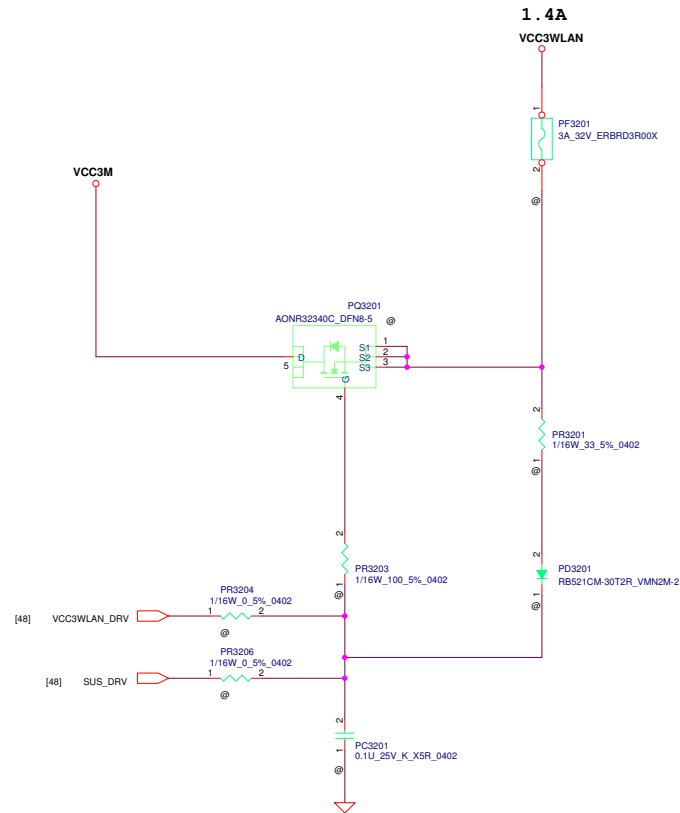







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